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# MS-7808

ATX  
Ver:0A

H/W:Frankyang  
PM:Feifei

## Intel -MahoBay plamform B75

### CPU:

IVY bridge LGA1155

### System Chipset:

Panther Point B75

### Onboard Chip:

Audio Codec: 887  
LAN-RTL8111E colay8105E  
SIO:Fintek F71868AD  
Flash ROM: SPI 128 MB

### Main Memory:

DDRIII (1066/1333/1600MHz) \* 2 (Dual Channel)

### ACPI:

UPI

### PWM:

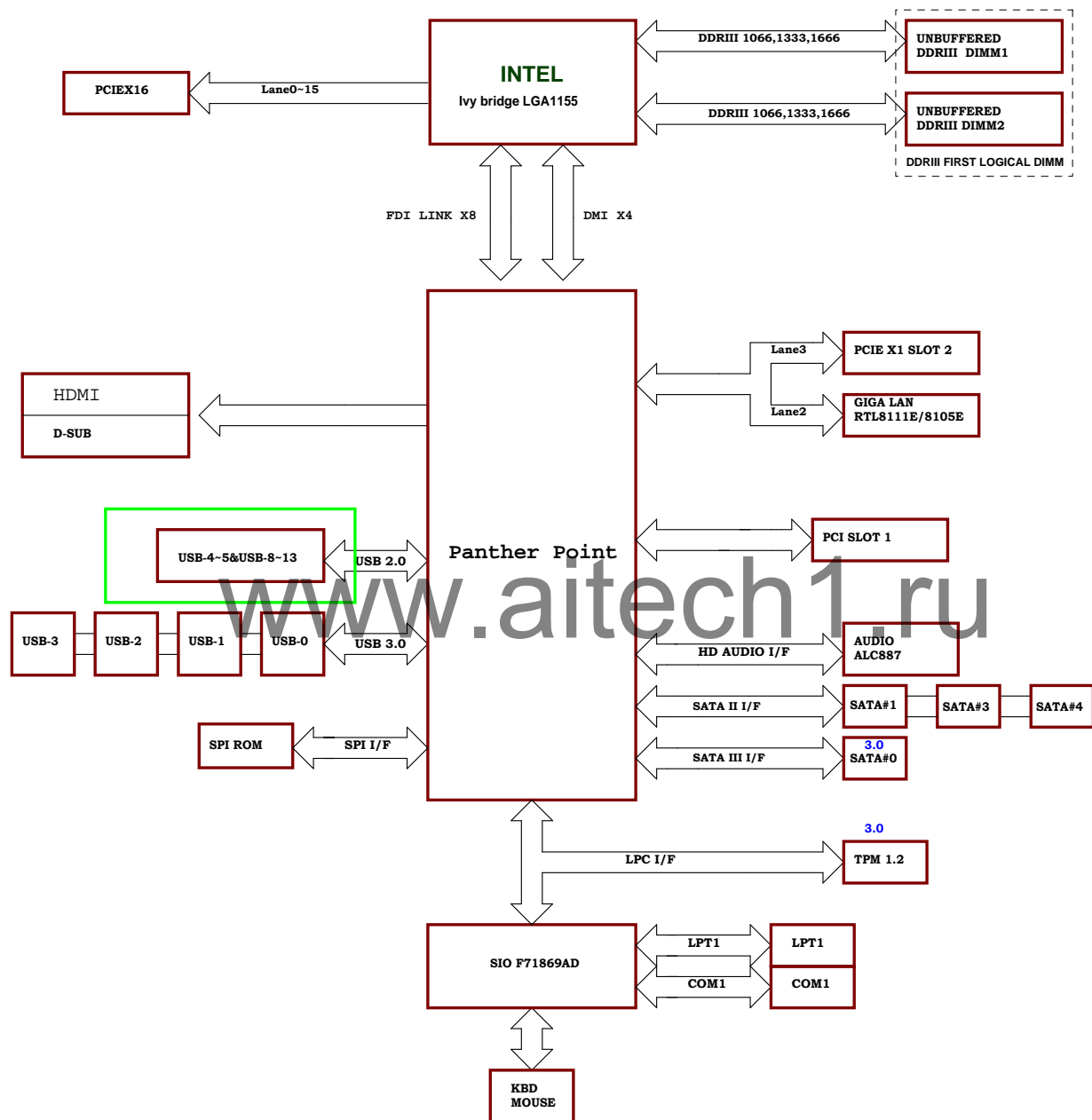
VRD12 -UT501 3+1 Phase

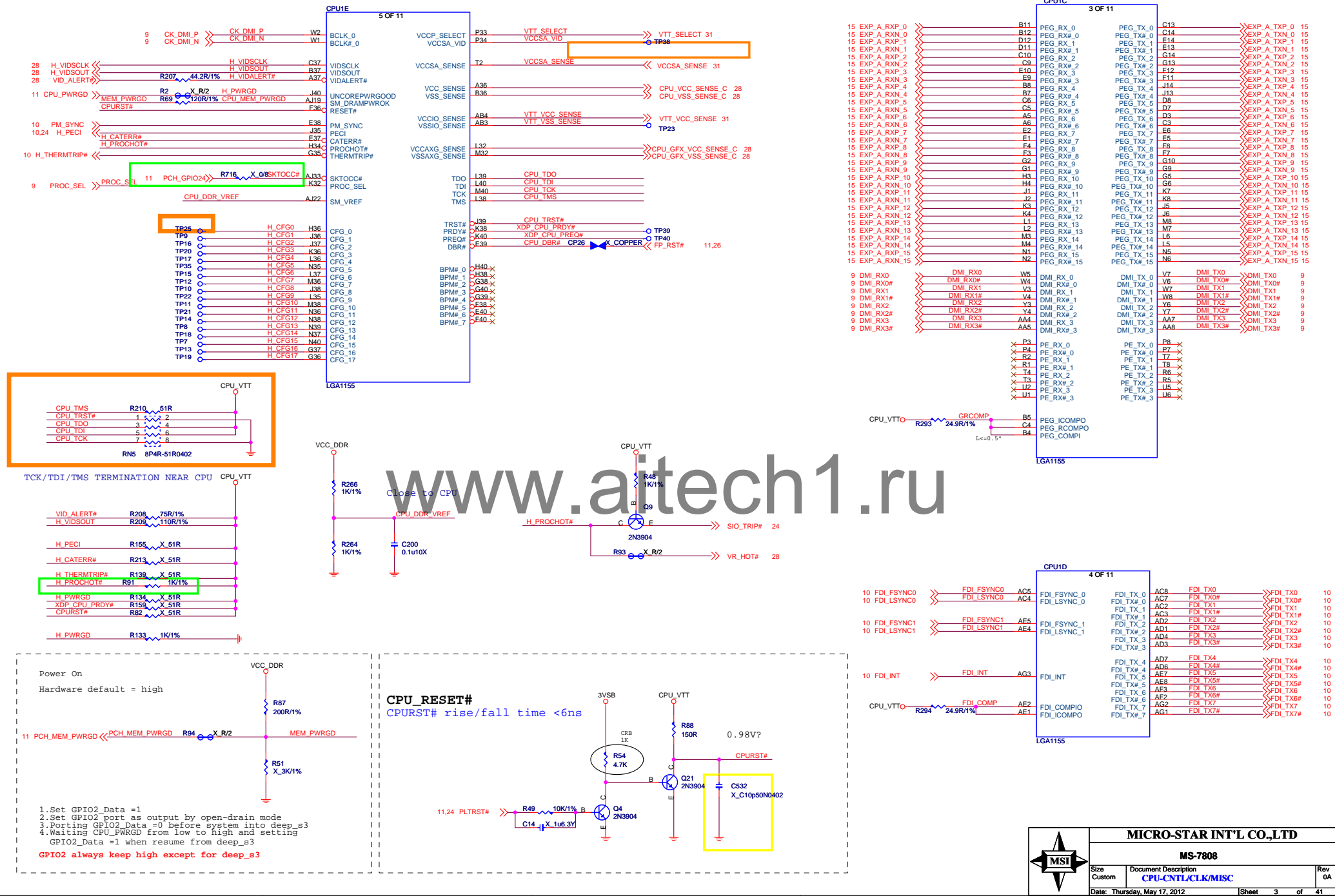
### Expansion Slots:

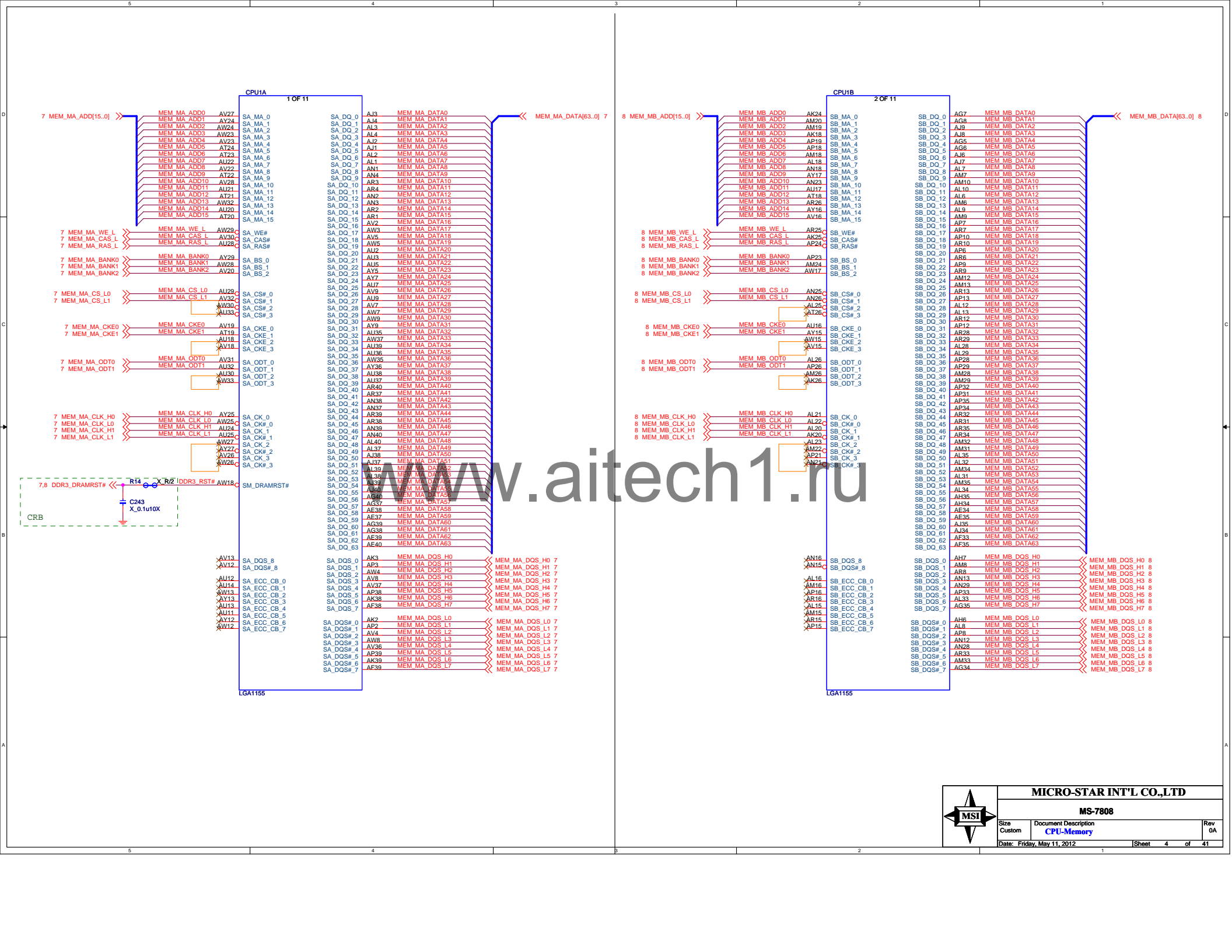
PCI Express (X16) Slot \* 1  
PCI Express (X1 ) Slot \* 1  
PCI Slot \* 1

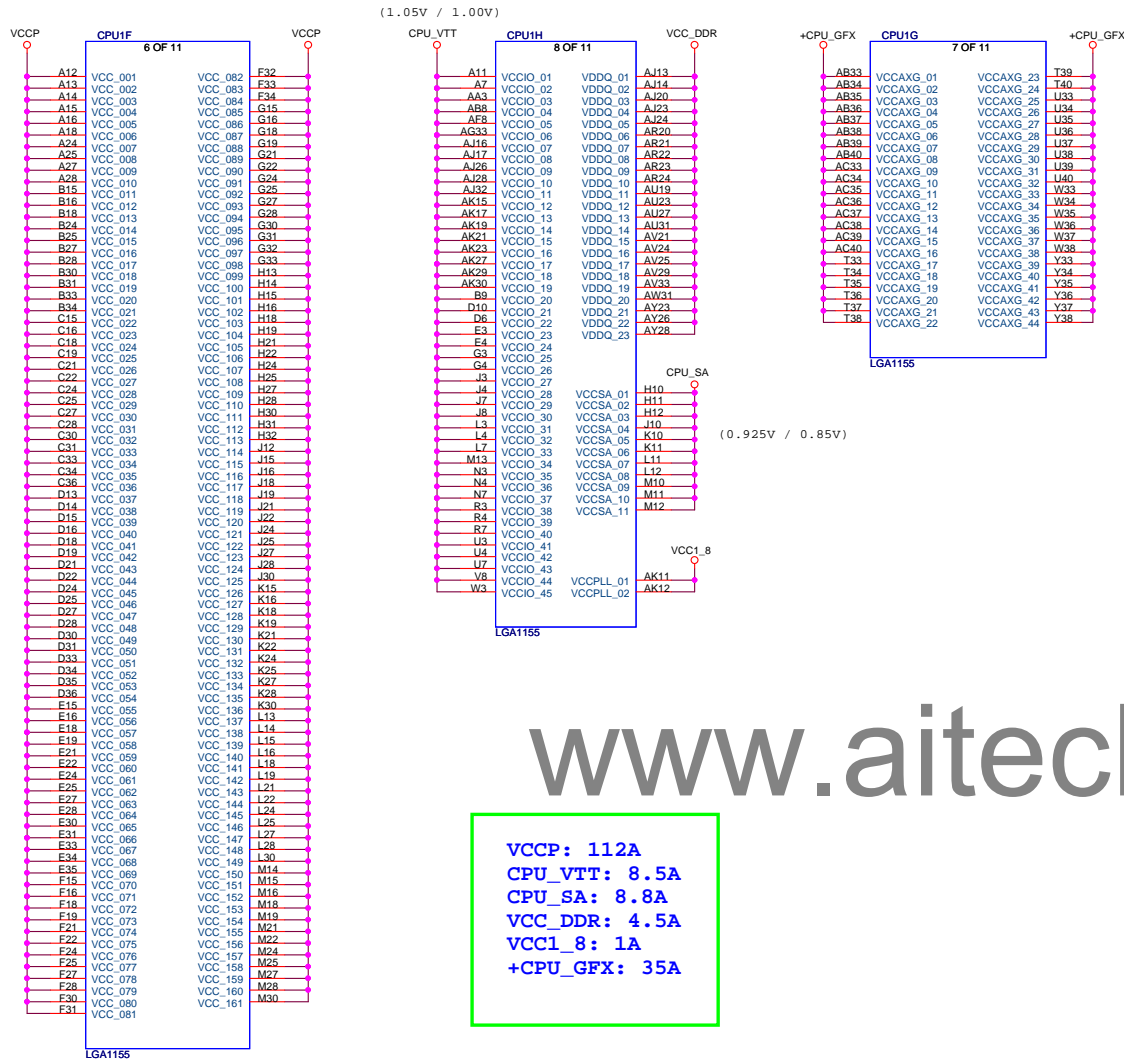
### Other: SATA3.0 x1+SATA2.0 x3 (PCH)

USB2.0 \*8  
REAL USB3.0 \*2  
FRONT USB3.0 \*2



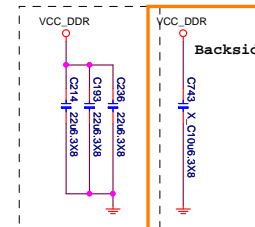






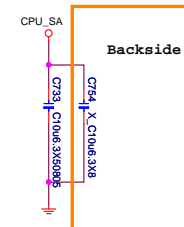
### +1.5V\_DDR3-Decoupling

CPU SOCKET CAVITY CAPS



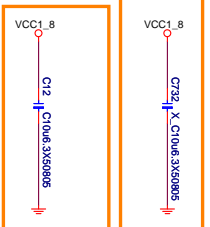
### +CPU\_SA Decoupling

Backside



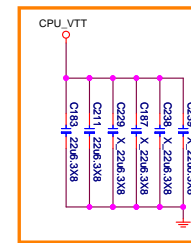
### +VCC1\_8 Decoupling

Backside

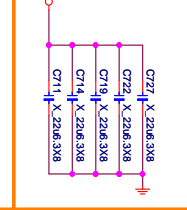


### +CPU\_VTT Decoupling

CPU SOCKET CAVITY CAPS

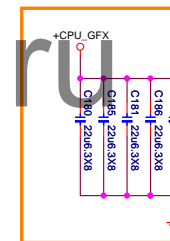


Backside

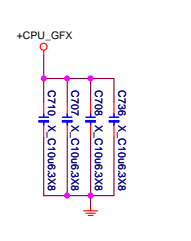


### +CPU\_GFX Decoupling

CPU SOCKET CAVITY CAPS

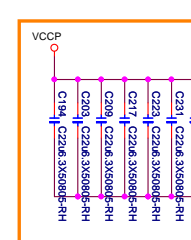


Backside

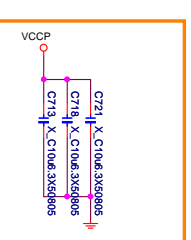


### +CPU\_VCCP-Decoupling

CPU SOCKET CAVITY CAPS



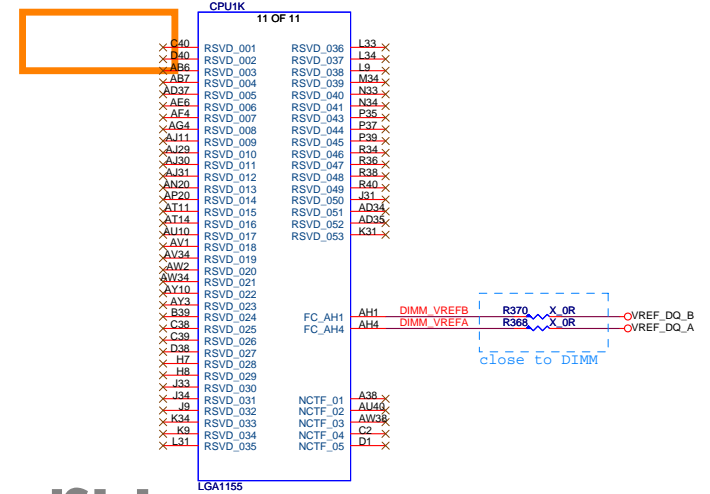
Backside



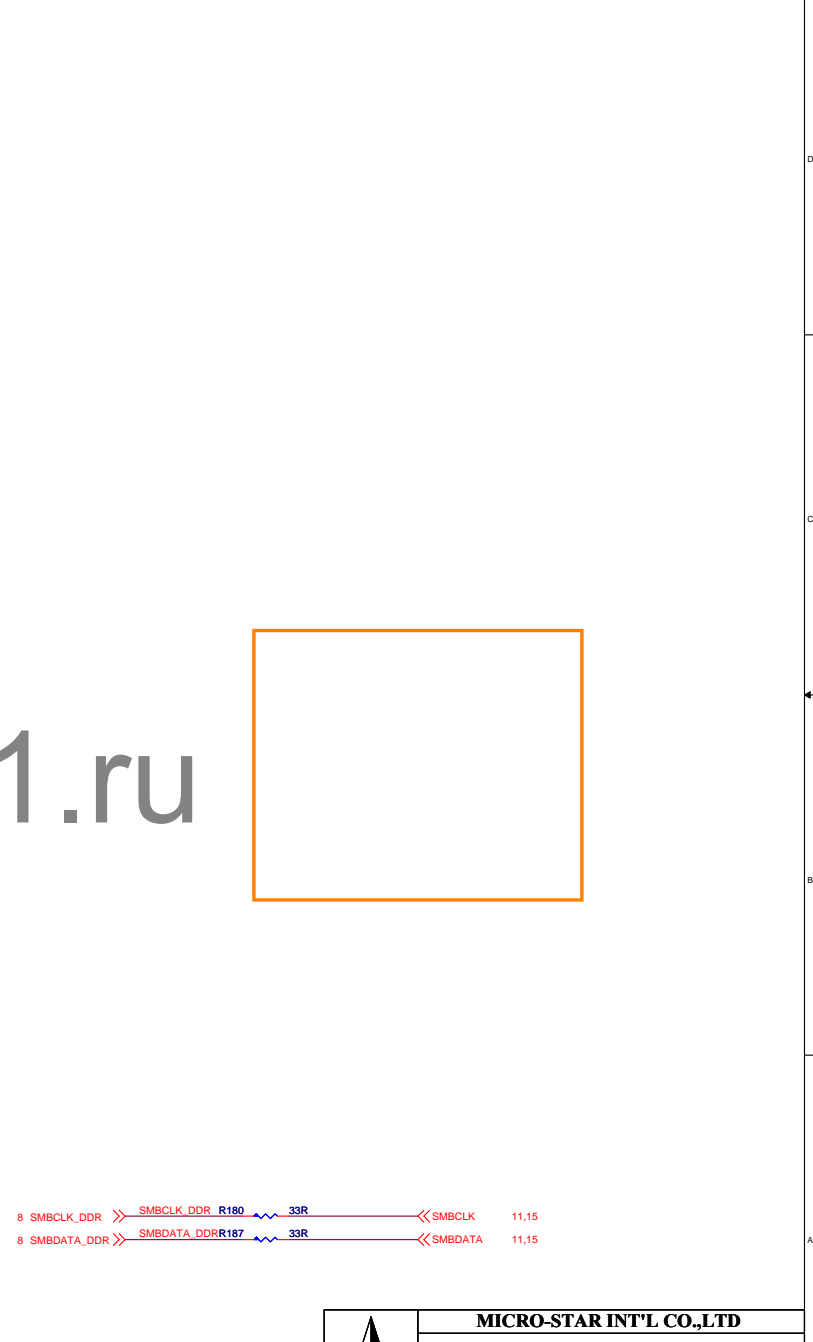
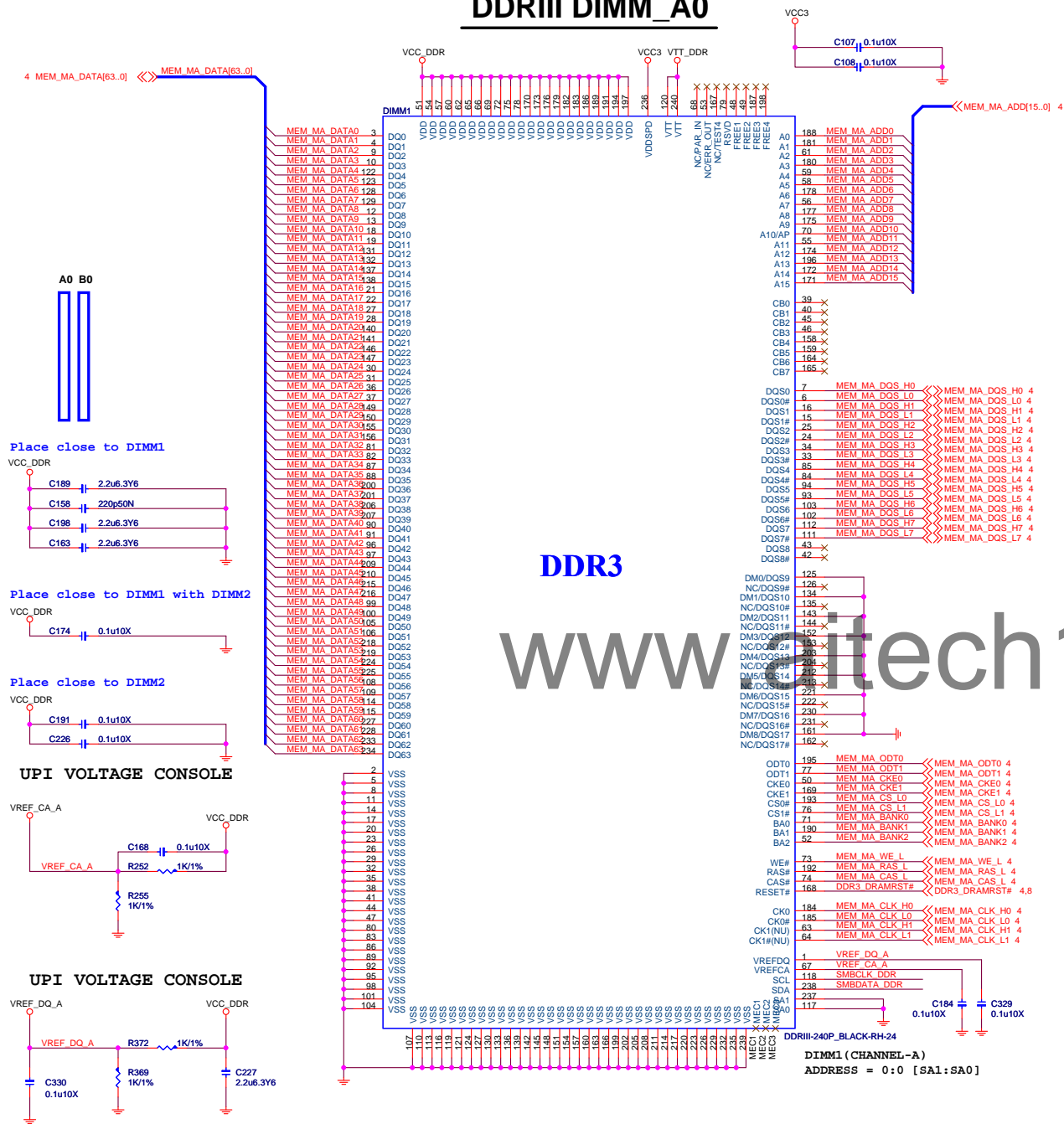
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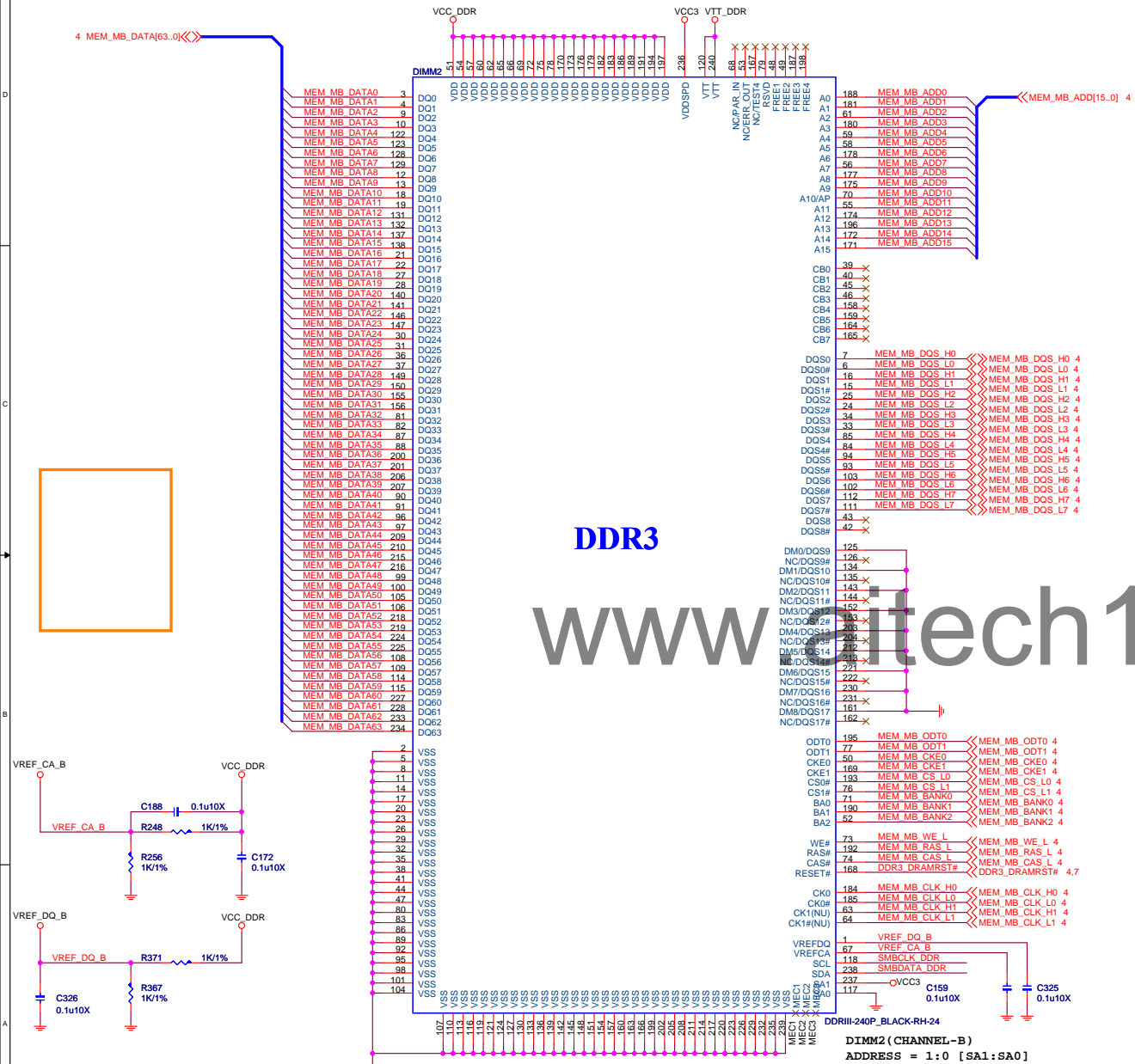
**MICRO-STAR INT'L CO.,LTD**

MS-7808

Size Custom	Document Description <b>DDR3 Chanel-A DIMM1/2</b>	Rev 0A
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# DDRIII DIMM\_B0



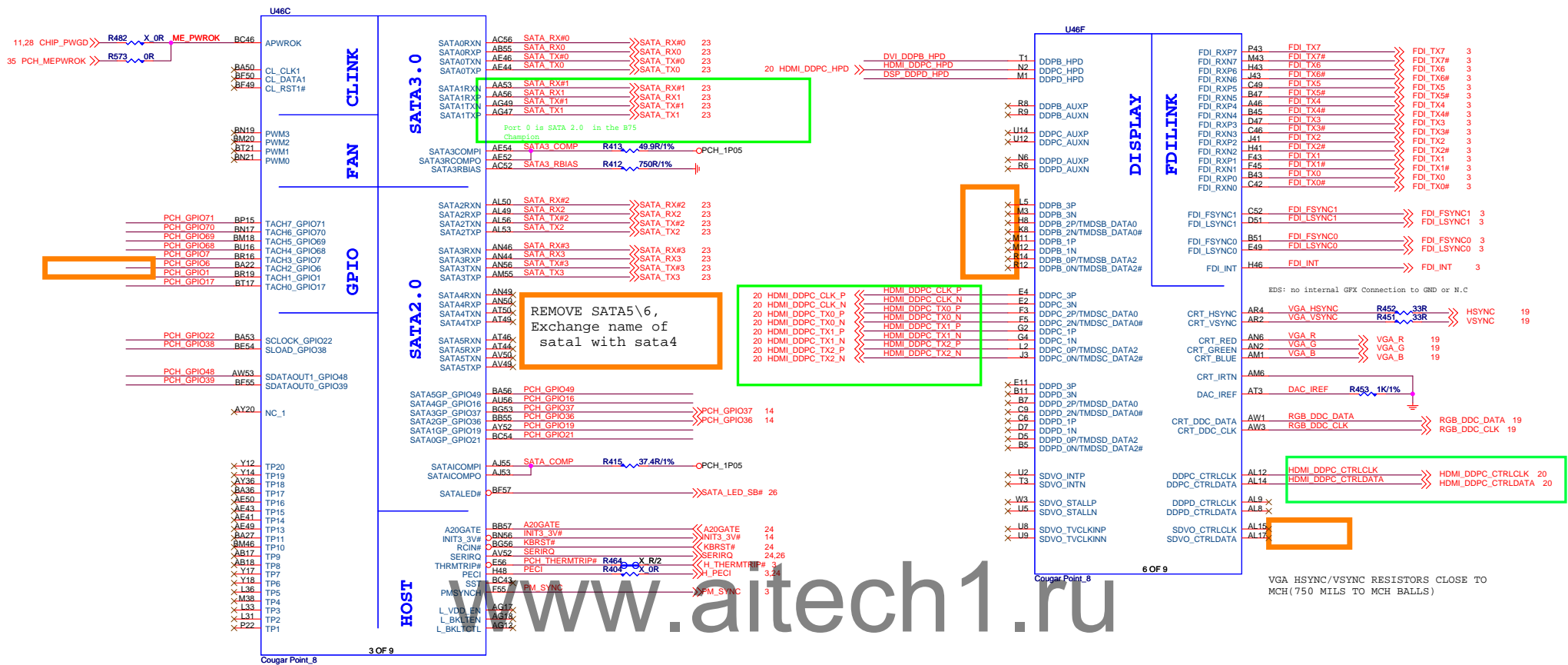
www.itech1.ru

SMBCLK\_DDR << SMBCLK\_DDR 7  
SMBDATA\_DDR << SMBDATA\_DDR 7

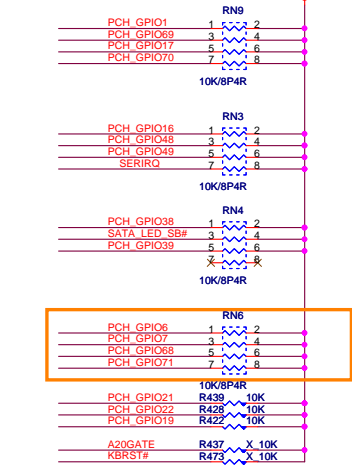
MICRO-STAR INT'L CO.,LTD			
MS-7808			
Size	Document Description	Rev	
Custom	DDR3 Channel-B DIMM3/4	0A	
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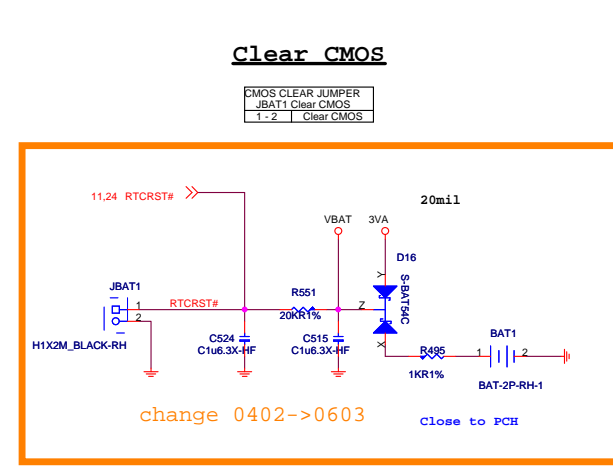




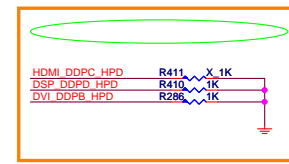
Pull HIGH for PCH



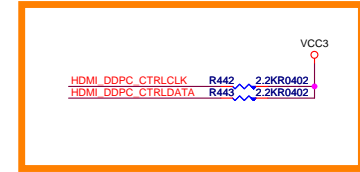
RTC and CLR\_CMOS



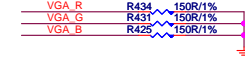
No Display port( pull down)



Enable VGA( CTRLCLK/DATA Pull High)



Close to PCH within 250 mils.

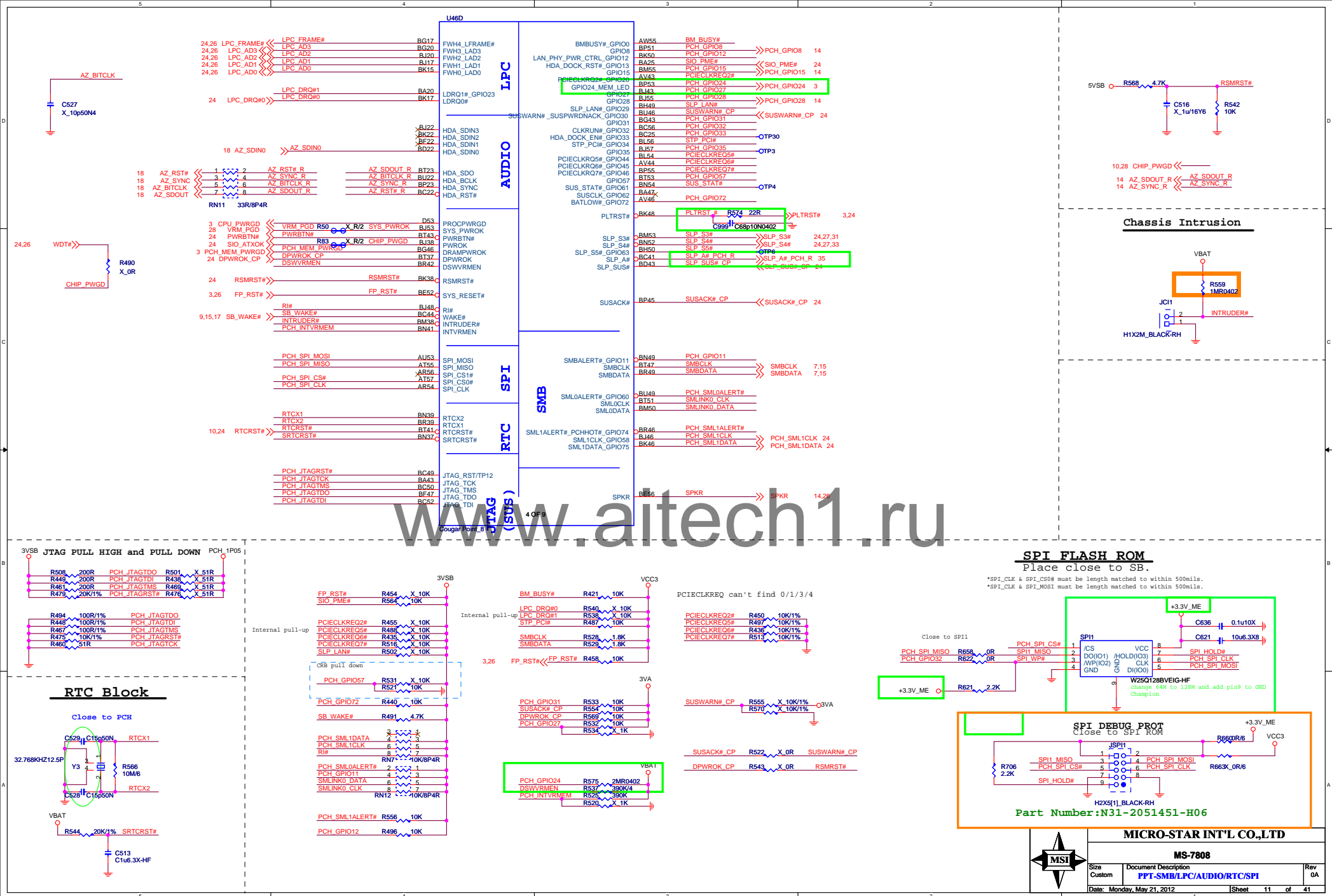


**MICRO-STAR INT'L CO.,LTD**

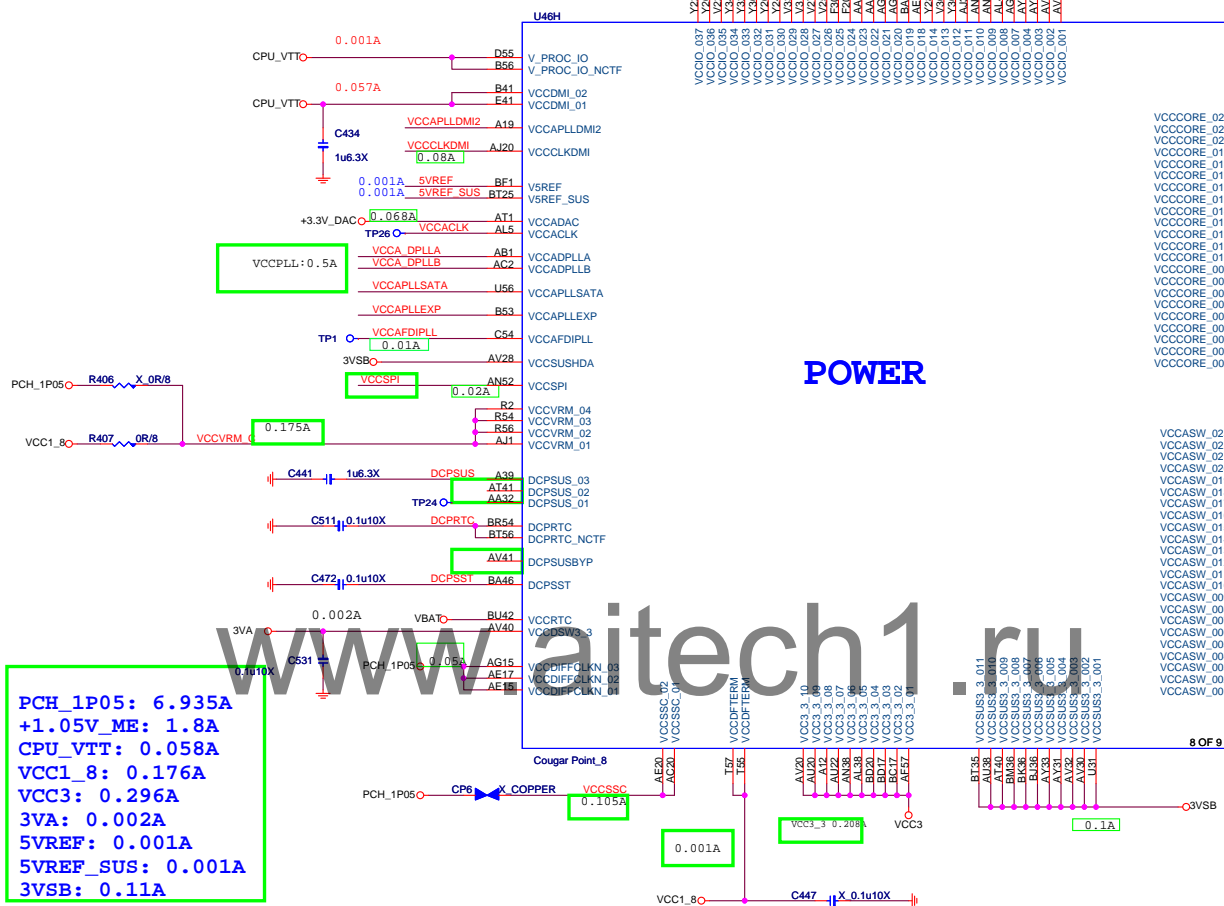
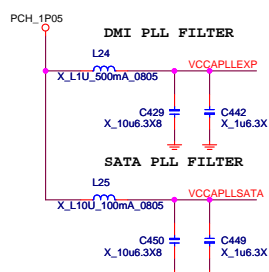
**MS-7808**

Size Custom Document Description PPT-SATA/HOST/GPIO/VGA/CCMOS Rev 0A

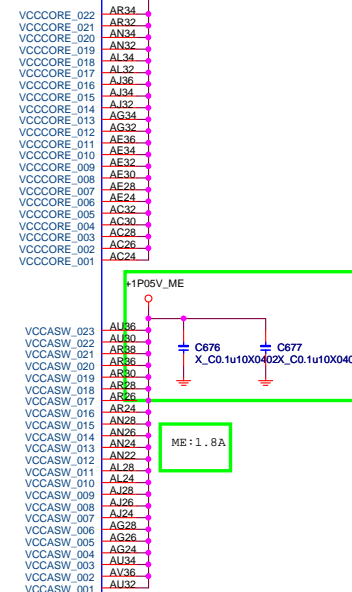
Date: Monday, May 21, 2012 Sheet 10 of 41



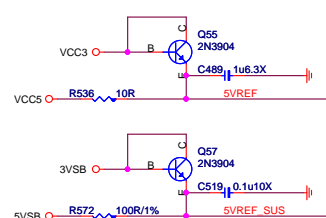
Change to 10UH if  
VCCA\_DPLLA/VCCA\_DPLLB  
has noise issue.



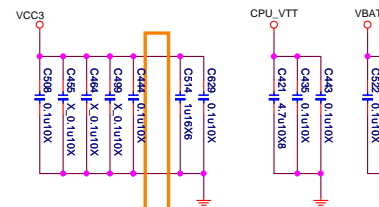
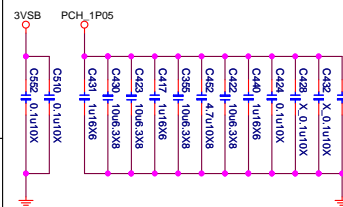
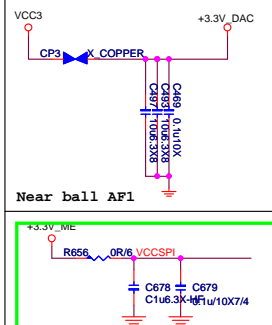
```
PCH_1P05: 6.935A
+1.05V_ME: 1.8A
CPU_VTT: 0.058A
VCC1_8: 0.176A
VCC3: 0.296A
3VA: 0.002A
5VREF: 0.001A
5VREF_SUS: 0.001A
3VSB: 0.11A
```



### 5VREF & 5VREF\_SUS Sequencing Circuit



PCH decoupling cap



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	Size
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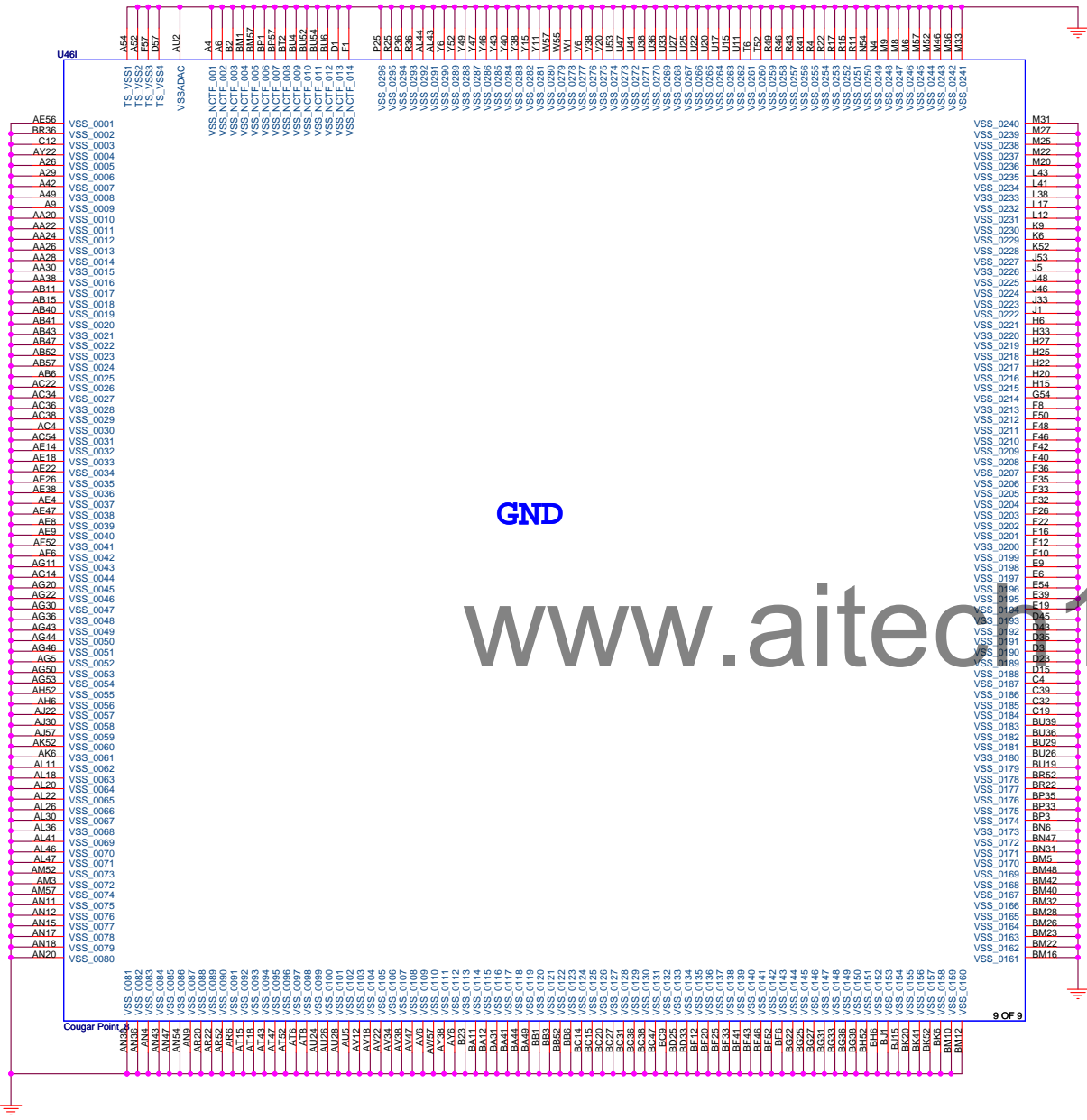
Document Description
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Custom

**PPT-POWER**

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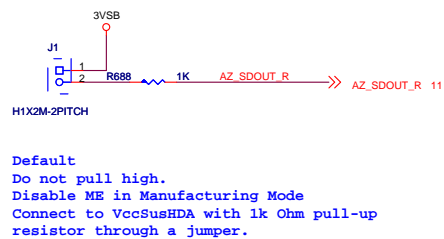
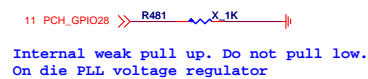
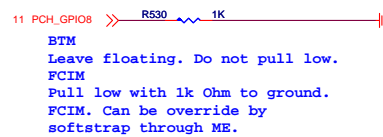
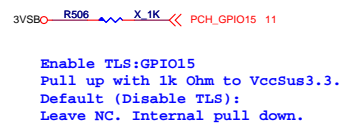
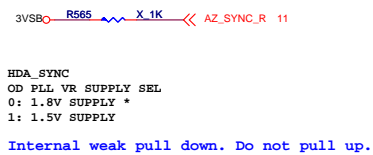
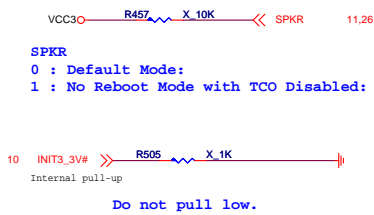


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PCH Straps



Since Pin has strap functionality that requires internal pull-down to be sampled at rising PWROK, following guidelines are required to be followed:

a) When Used as SATA2GP/SATA3GP for Mechanical Presence detect - Use a weak external pull-up (150K-200K ohms) to Vcc3.3 OR use 10K external pull-up that is enabled only after PLTRST# de-assertion.

b) When Used as GP Input (Pin HW default) Ensure GPI is not driven high during strap sampling window  
When Unused as GPIO or SATA[x]GP Use 8.2K-10K pull-down to ground.



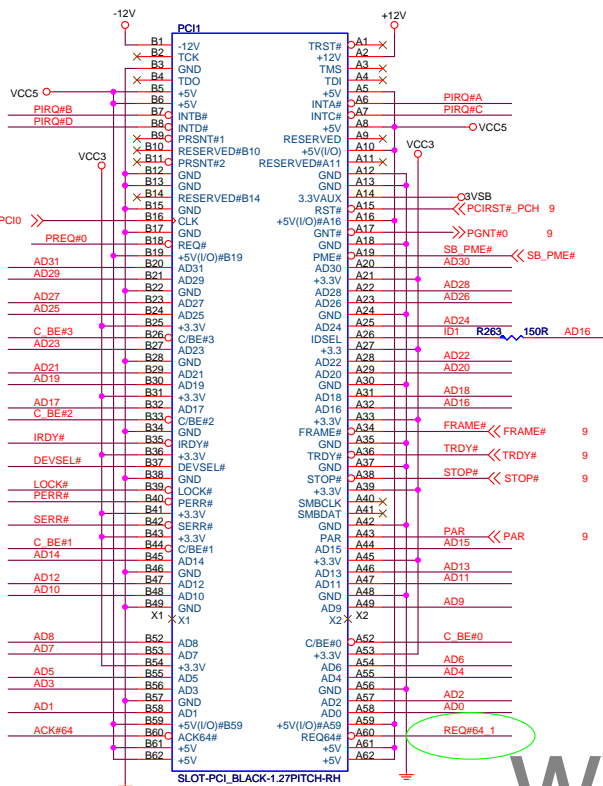
Since Pin has strap functionality that requires internal pull-down to be sampled at rising PWROK, following guidelines are required to be followed:

a) When Used as SATA2GP/SATA3GP for Mechanical Presence detect - Use a weak external pull-up (150K-200K ohms) to Vcc3.3 OR use 10K external pull-up that is enabled only after PLTRST# de-assertion.

b) When Used as GP Input (Pin HW default) Ensure GPI is not driven high during strap sampling window  
When Unused as GPIO or SATA[x]GP Use 8.2K-10K pull-down to ground.





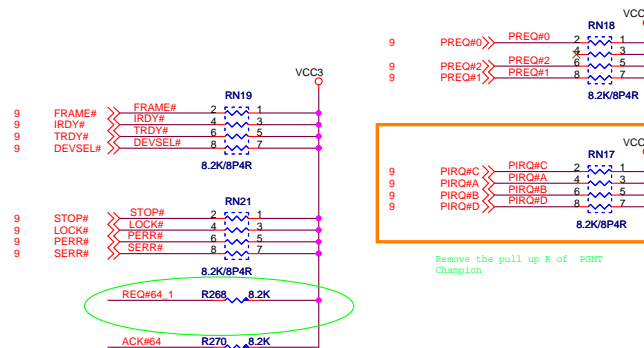
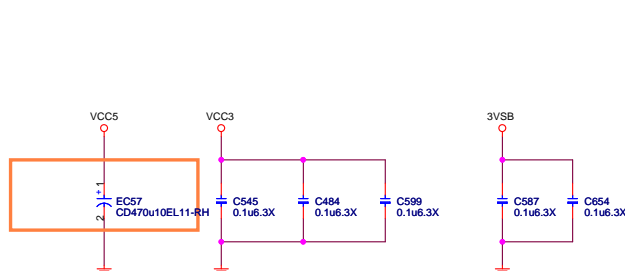


**IDSEL = AD16**  
**MASTER = PREQ#0**  
**PIRQ#A**

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AD[31..0] <<> AD[31..0] 9  
 C\_BE[3..0] <<> C\_BE[3..0] 9

#### PCI PULL-UP / DOWN RESISTORS



Remove the pull up R of PERR#  
Champion

#### PCI slot

+3.3Vaux	- 375mA
+3.3V	- 7.6A
+12V	- 0.5A

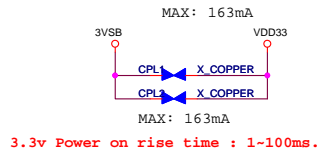
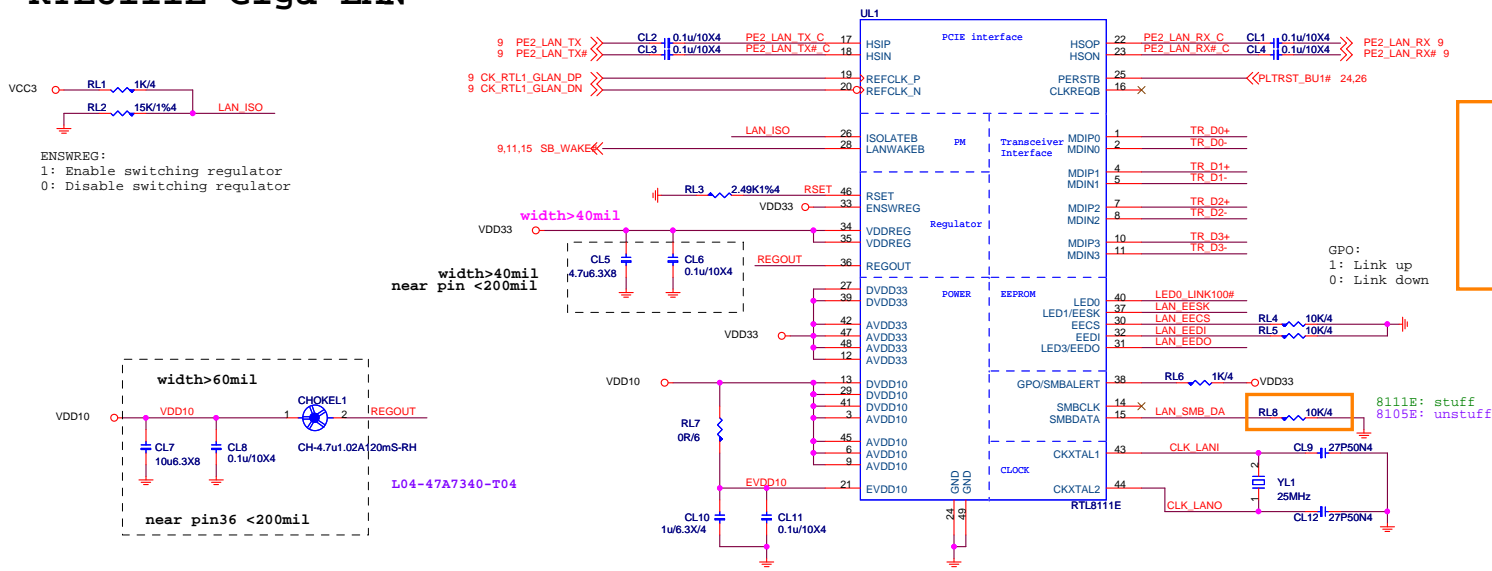


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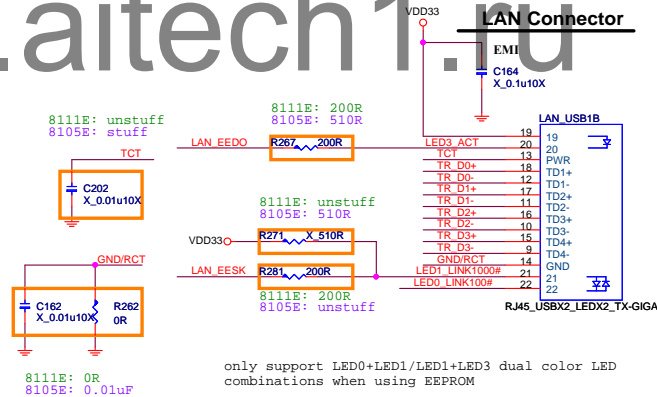
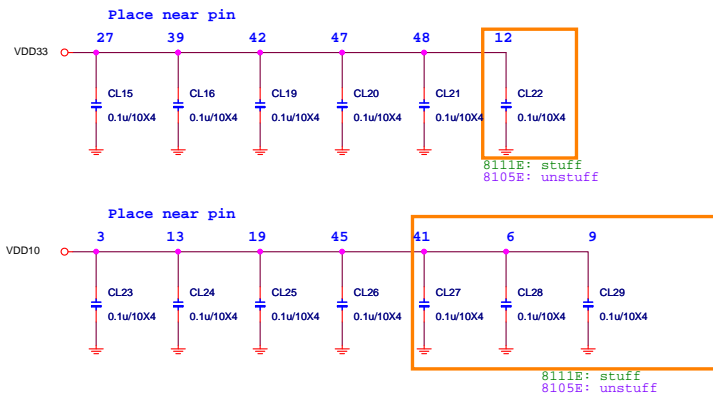
Size Custom	Document Description PC1x1 Slots	Rev 0A
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# RTL8111E Giga LAN



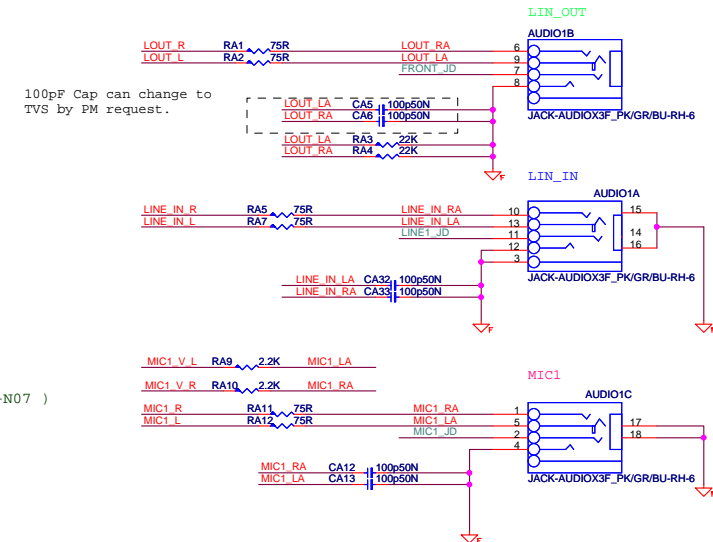
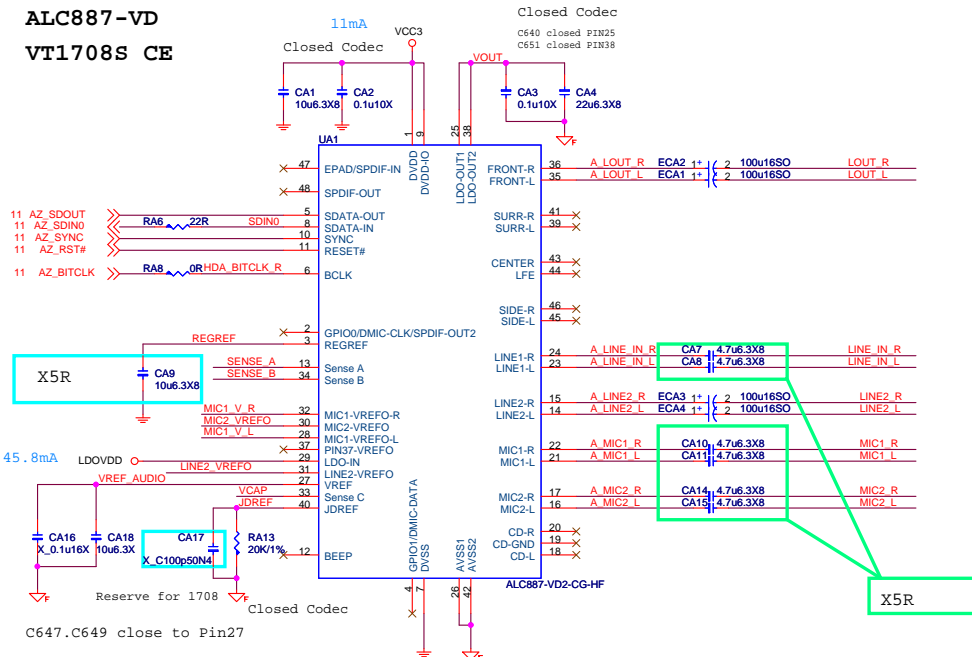
8111E POWER Consumption

	3.3V	100M
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13

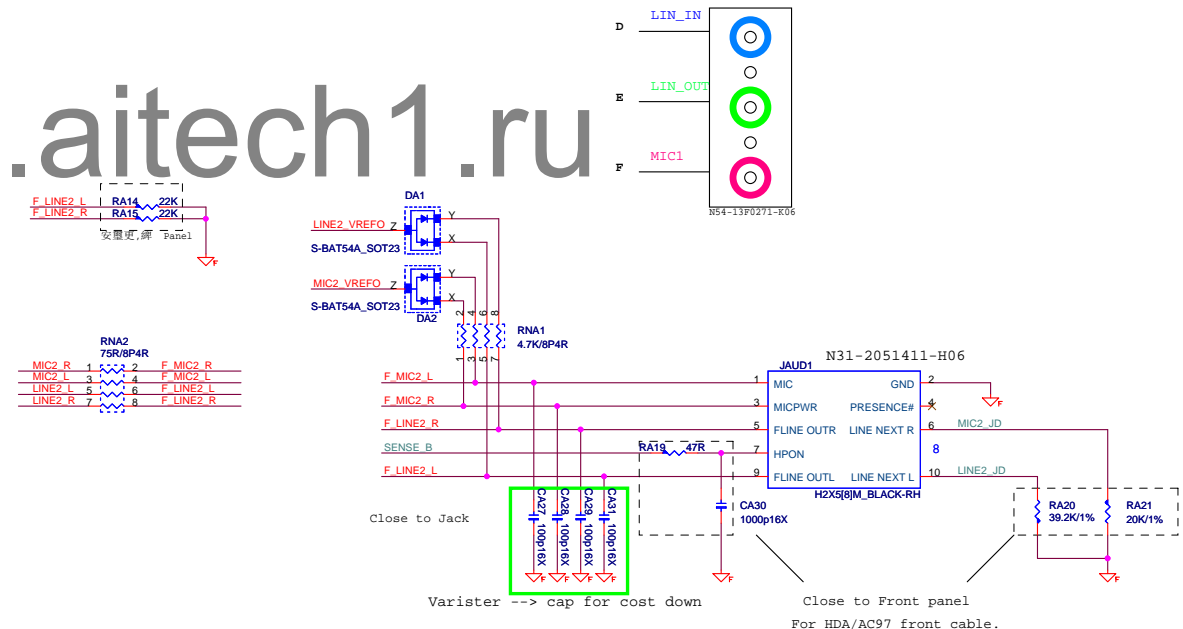
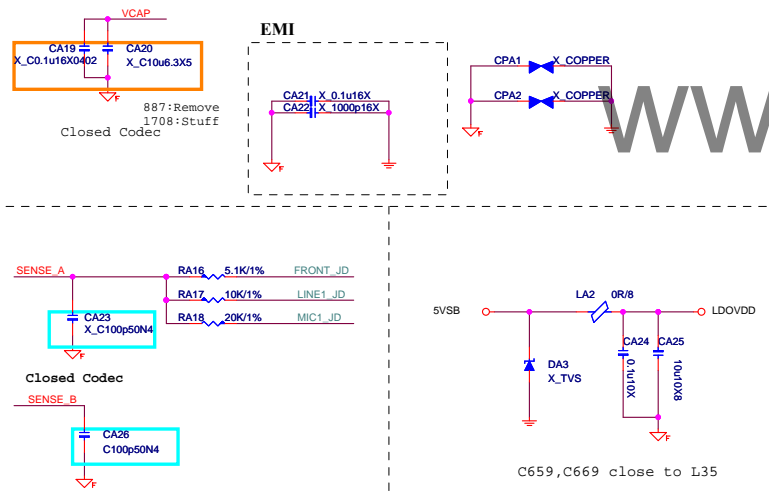


Giga-Lan	10/100-Lan
N58-22F0731	N58-22F0771
Link Yellow	Link Yellow
Active Blinking 1000	Active Blinking 100
Active Blinking 100	Active Blinking 100
None	None

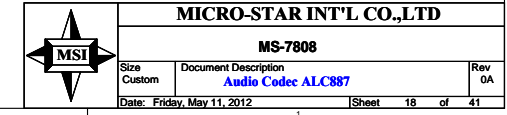
ALC887-VD  
VT1708S CE



EL 100u ( C94-1012511-N07 )



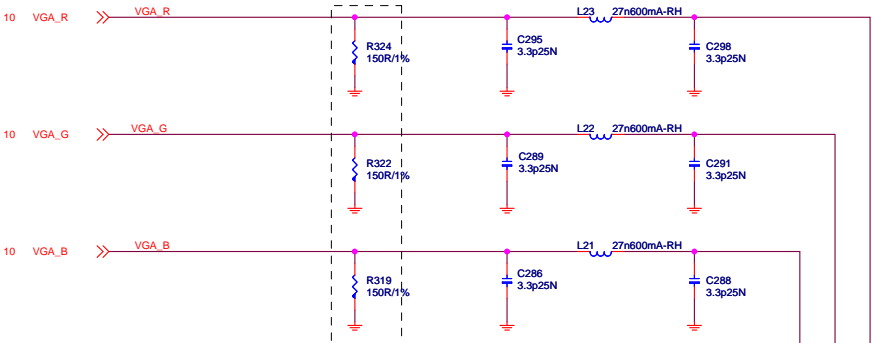
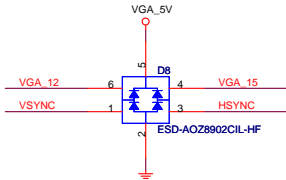
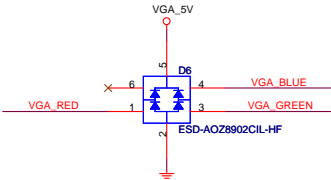
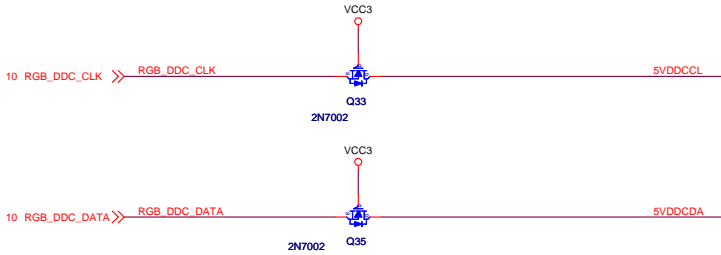
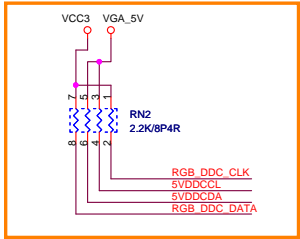
SPDIF OUT



D-Sub

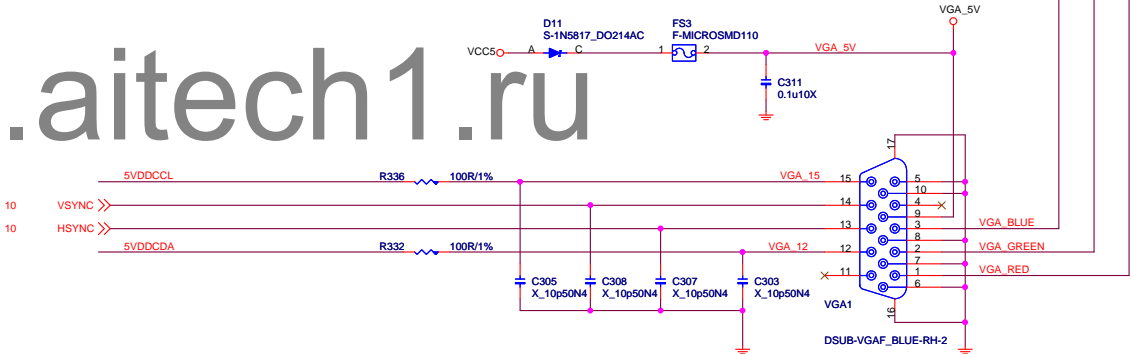
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

Level shift



PLACE CLOSE TO VGA CONNECTOR,  
WITHIN 750 MIL OF PIN

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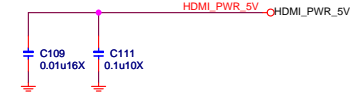
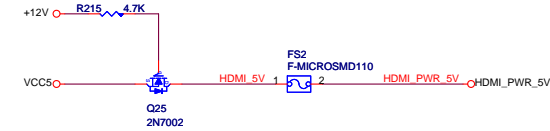
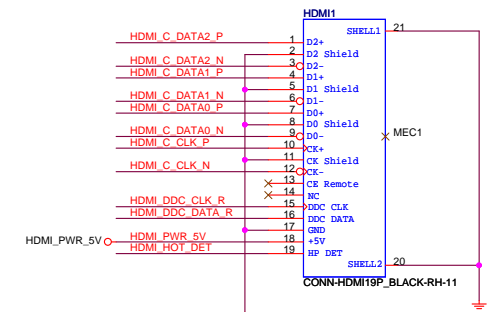
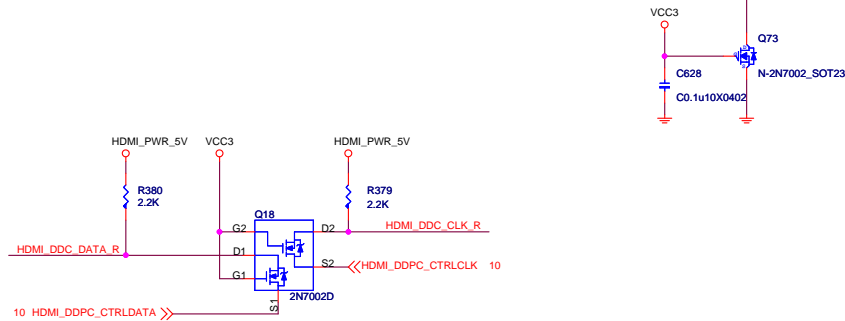
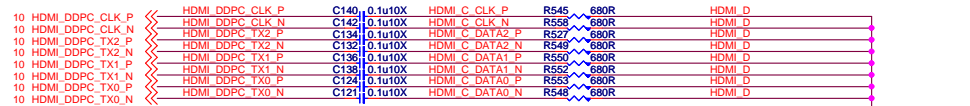


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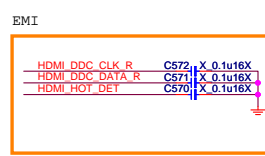
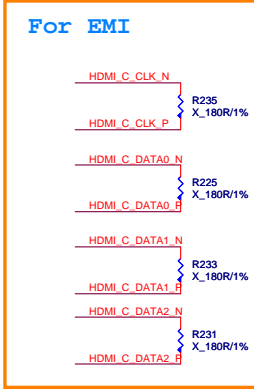
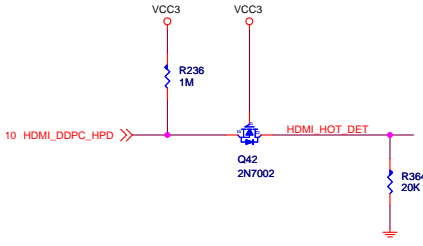
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		VGA Connector	0A
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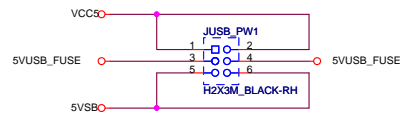
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)



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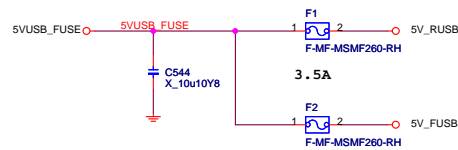


# 5V\_RUSB Switch

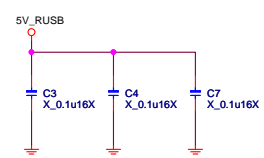
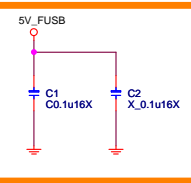


Default VCC5 (PIN1-3,2-4)

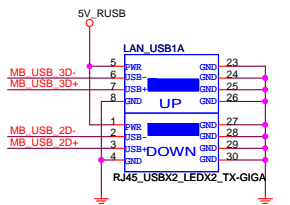
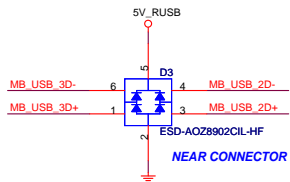
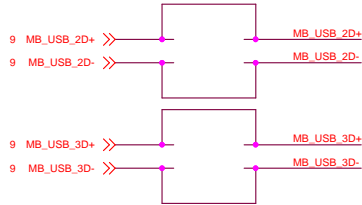
5V\_RUSB must 120mm



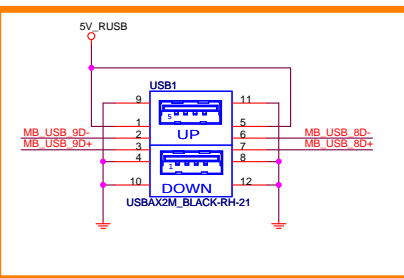
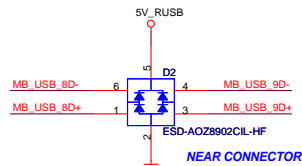
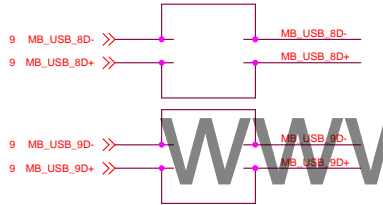
JUSB_PW1	BIOS Menu	Wake up support
1-3,2-4	EUP Enable	Not support
	EUP Disable	Not support
3-5,4-6	EUP Enable	Not support
	EUP Disable	support



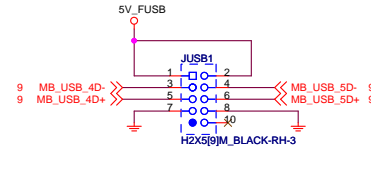
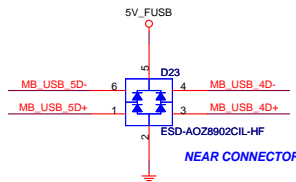
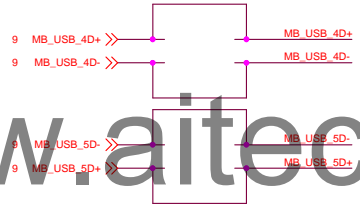
## REAR USB PORT 8,9 (With LAN)



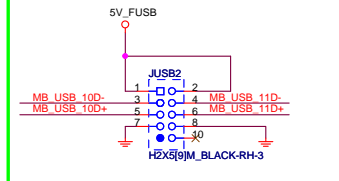
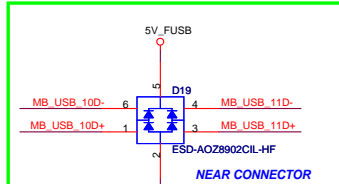
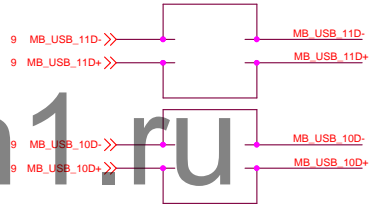
## REAR USB PORT 8,9 (USB1)



## FRONT USB PORT 0,1



## FRONT USB PORT 8,9



Remove USB2.0 PORT 10,11  
USB6&USB7  
Champion



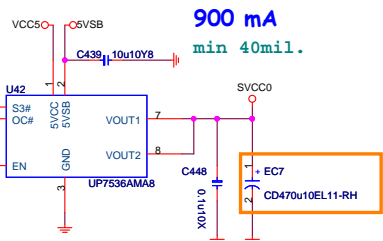
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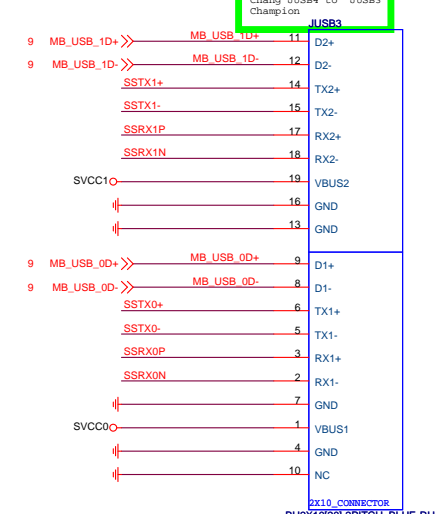
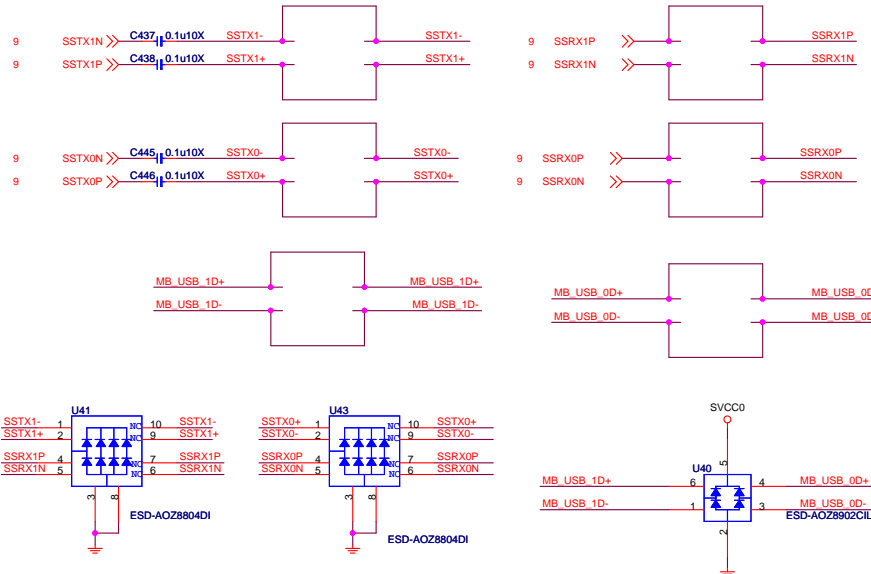
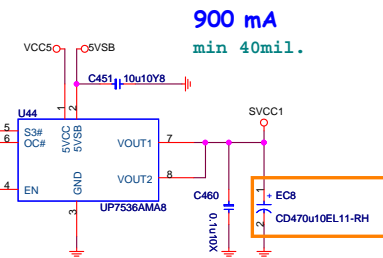
Size	Document Description	Rev
Custom	Rear I/O & USB2.0 Connector	0A
Date: Wednesday, May 23, 2012	Sheet 21 of 41	

# FRONT USB30 PORT 0,1

Same as SLP\_S3#

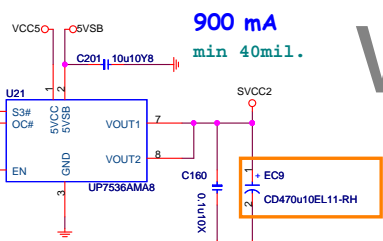


Same as SLP\_S3#

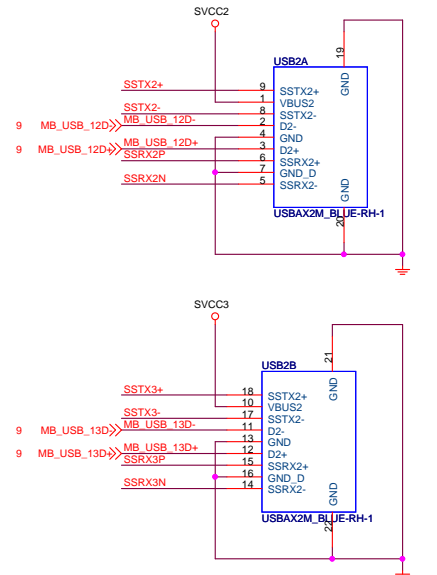
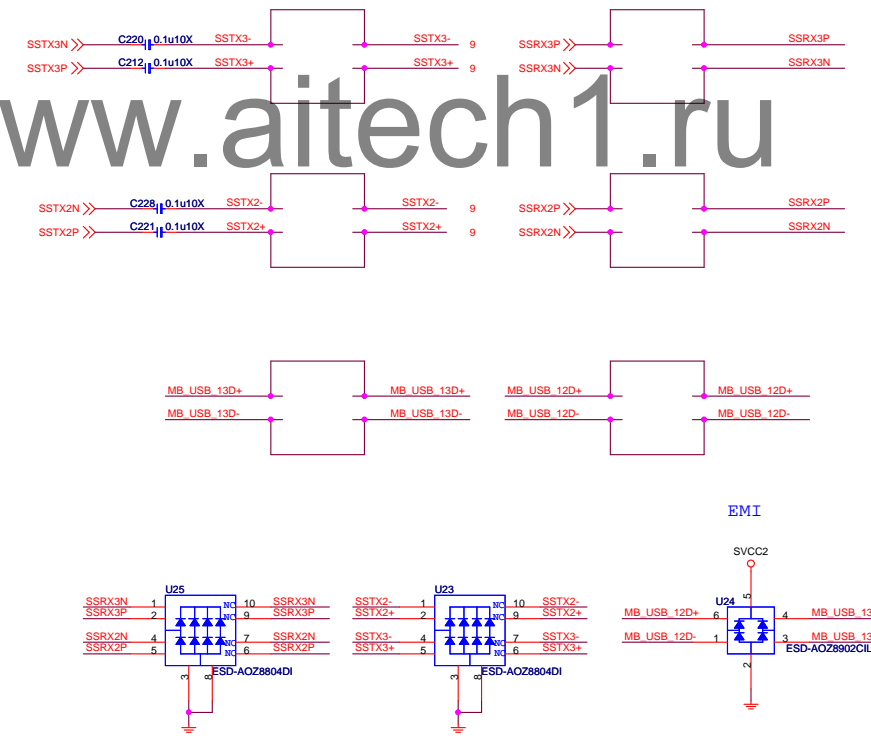
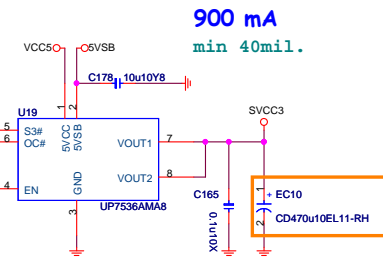


# REAR USB30 PORT 2,3

Same as SLP\_S3#



Same as SLP\_S3#



USB\_MODE  
Hi by BIOS programming,  
default h/w PD for avoid UP7536 Enable pin floating

USB_MODE States					
MODE	G3	S4/S5	S0	S3	
EUP Disable	0	0	1	1	
EUP Enable	0	0	1	1	

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**MS-7808**

Size Custom Document Description **USB3.0 Connector** Rev 0A

Date: Monday, May 21, 2012 Sheet 22 of 41



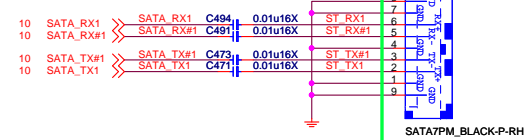
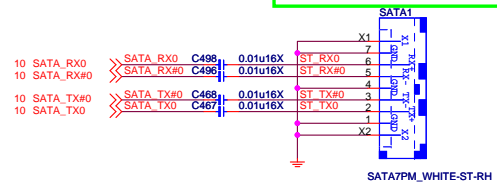
Change SATA5G PORT0,1 to SATA PORT 0

**SATA 6G PORT 0**

3.0 white

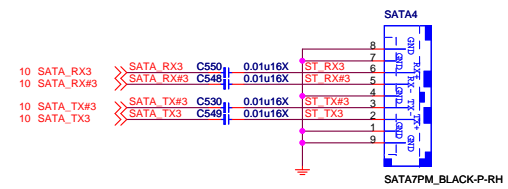
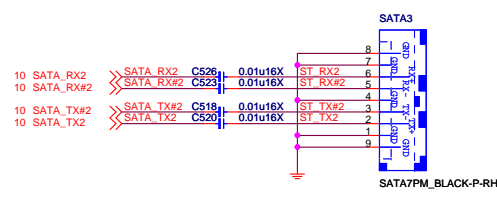
add SATA 3G PORT 1  
Champion

**SATA 3G PORT 1**



change SATA3.0 to SATA 2.0  
Champion

**SATA 3G PORT 2,3**

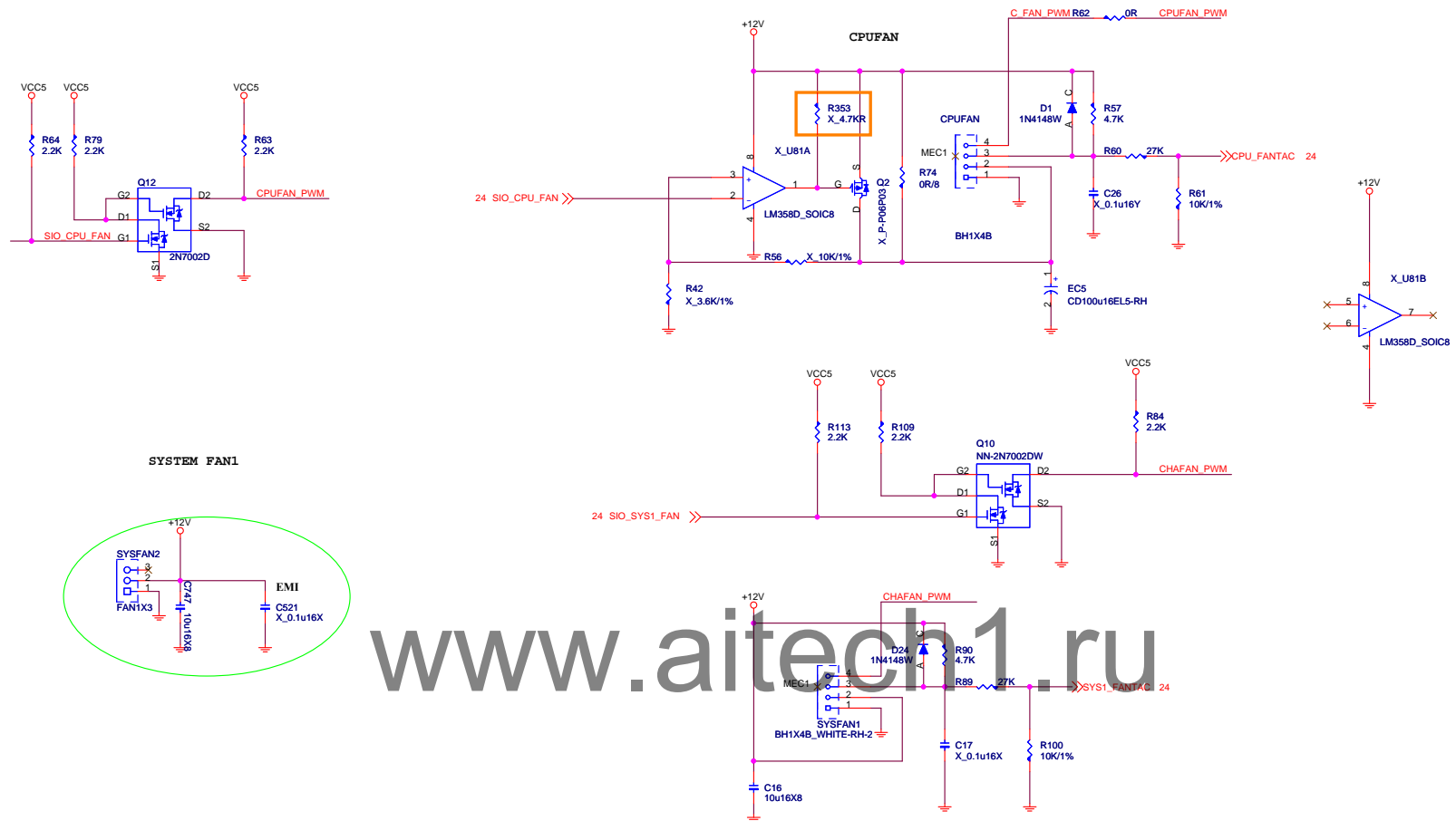


REMOVE SATA5\6 Exchange name of sata1 with sata4

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# FAN-COUNTROL CIRCUIT



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Size  
Custom

Document Description  
FAN Control

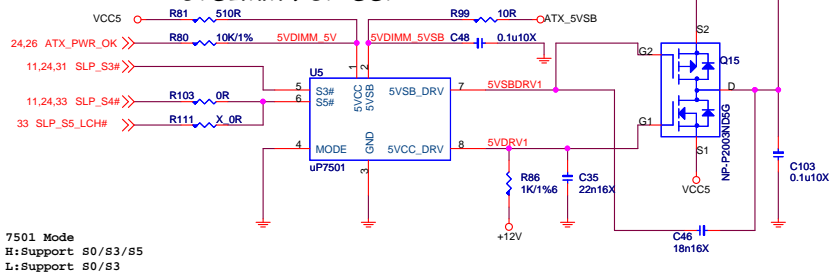
Date: Friday, May 11, 2012

Rev  
0A

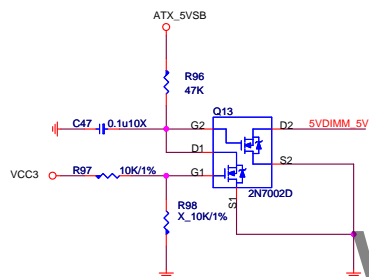
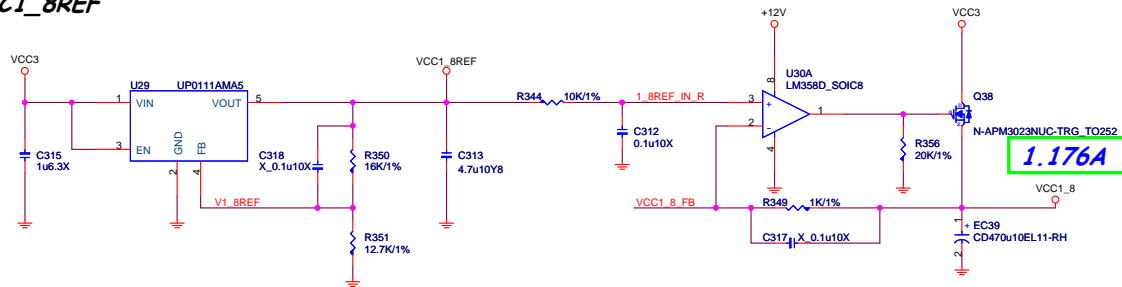
Sheet 25 of 41



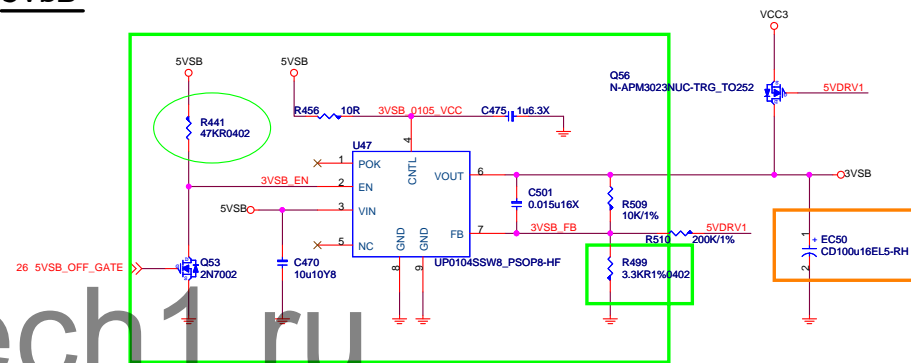
## 5VDIMM FOR DDR



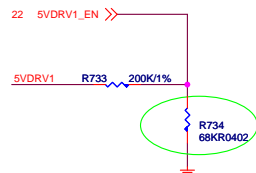
## VCC1\_8REF



## 3VSB

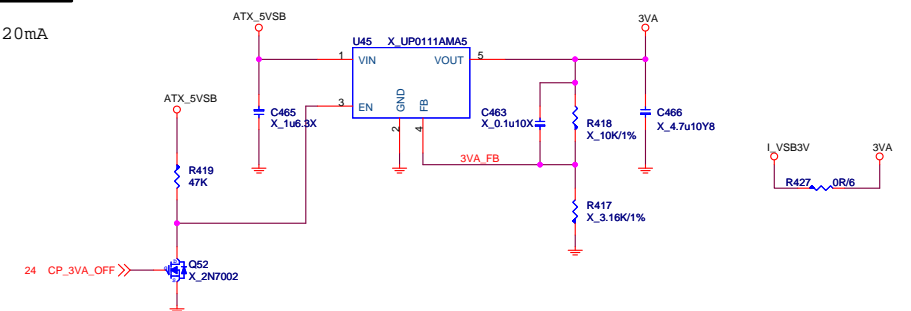


## USB MODE



## 3VA

20mA

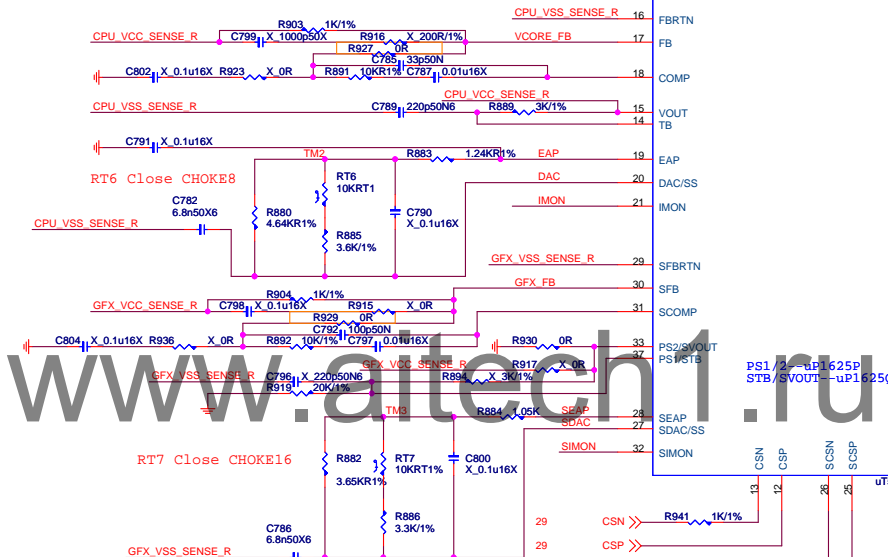
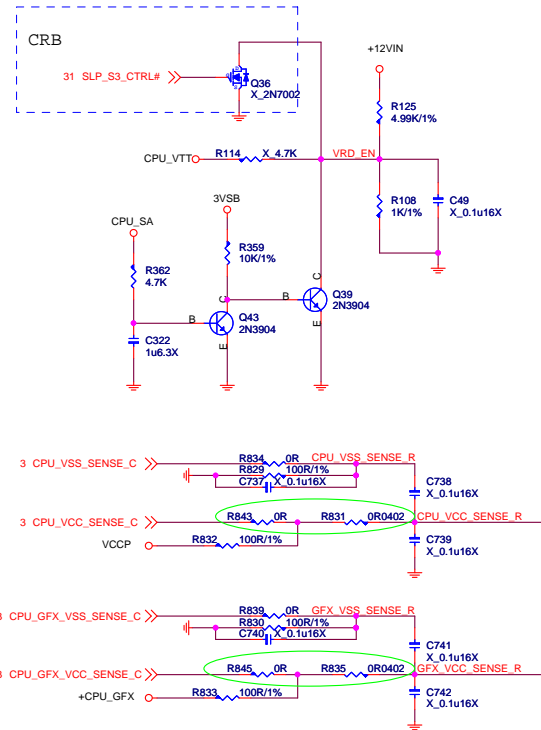
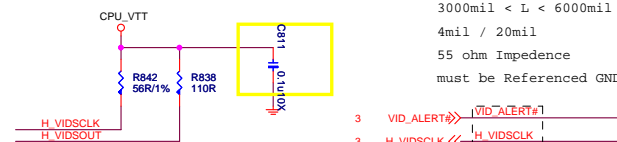
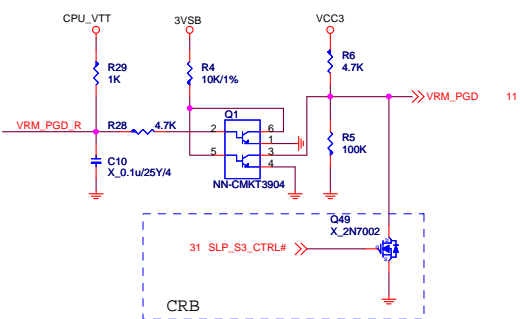


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Size	Document Description	Rev
Custom	ACPI controller UPI	0A
Date: Friday, May 11, 2012	Sheet 27 of 41	

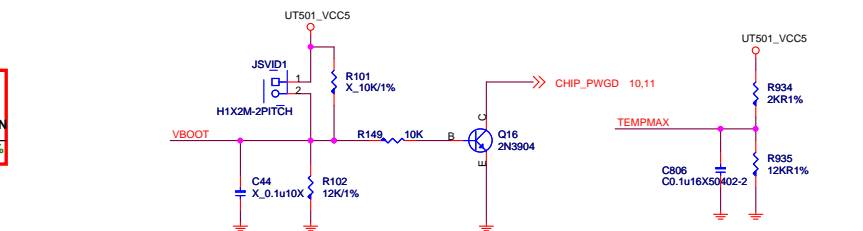
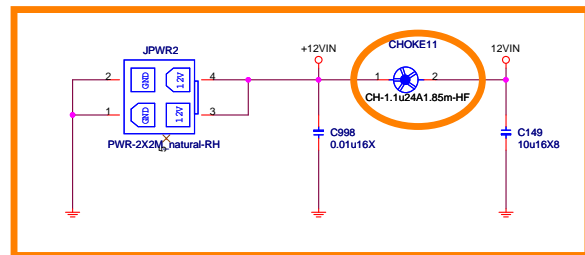
# VRMPWRGD LEVEL SHIFT



## UPI VOLTAGE CONSOLE

0x20: RH=10K, RL=OPEN

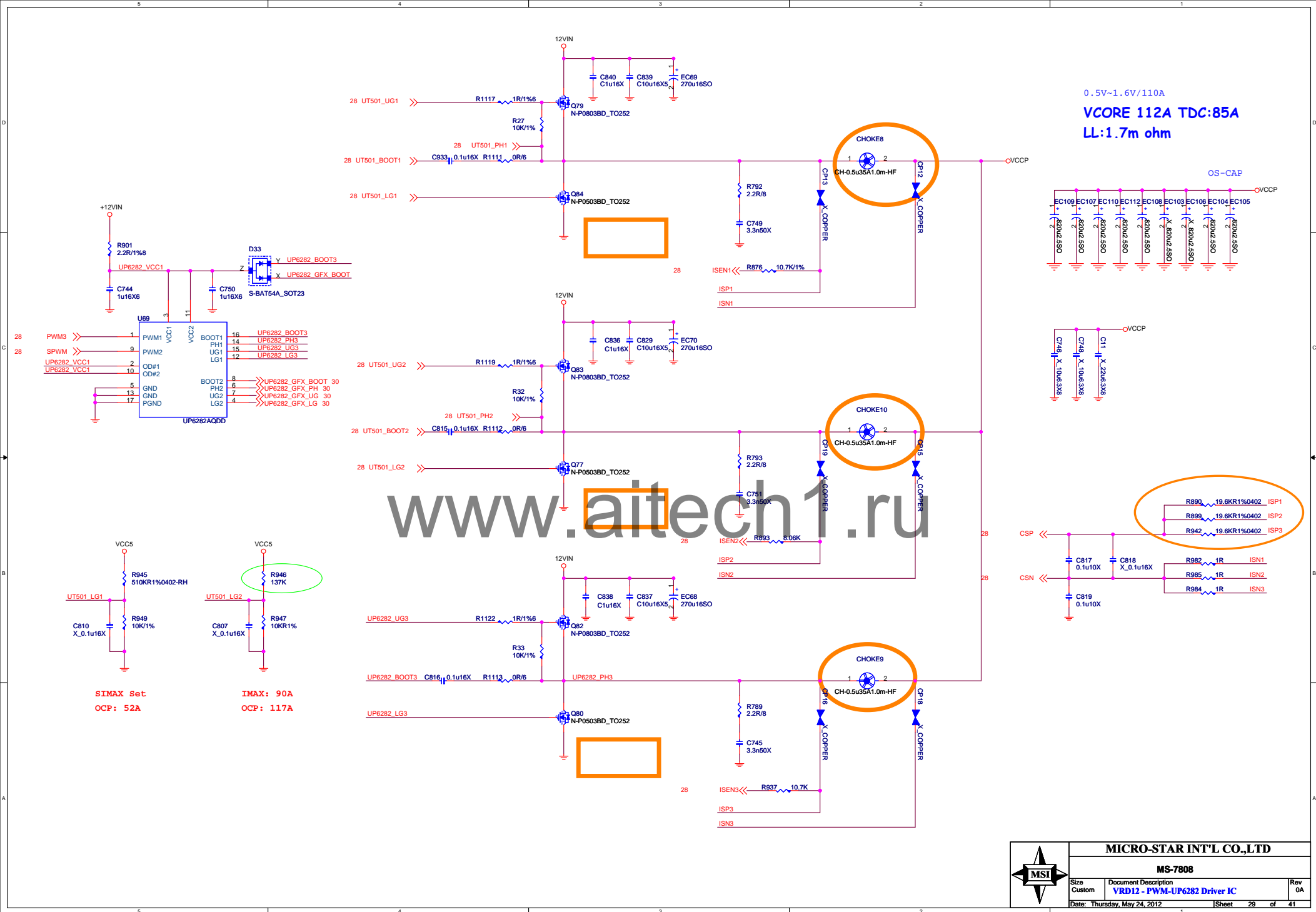
ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (Kohm)	OPEN	3.9	3	2.2	1.3	10
RL (Kohm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%



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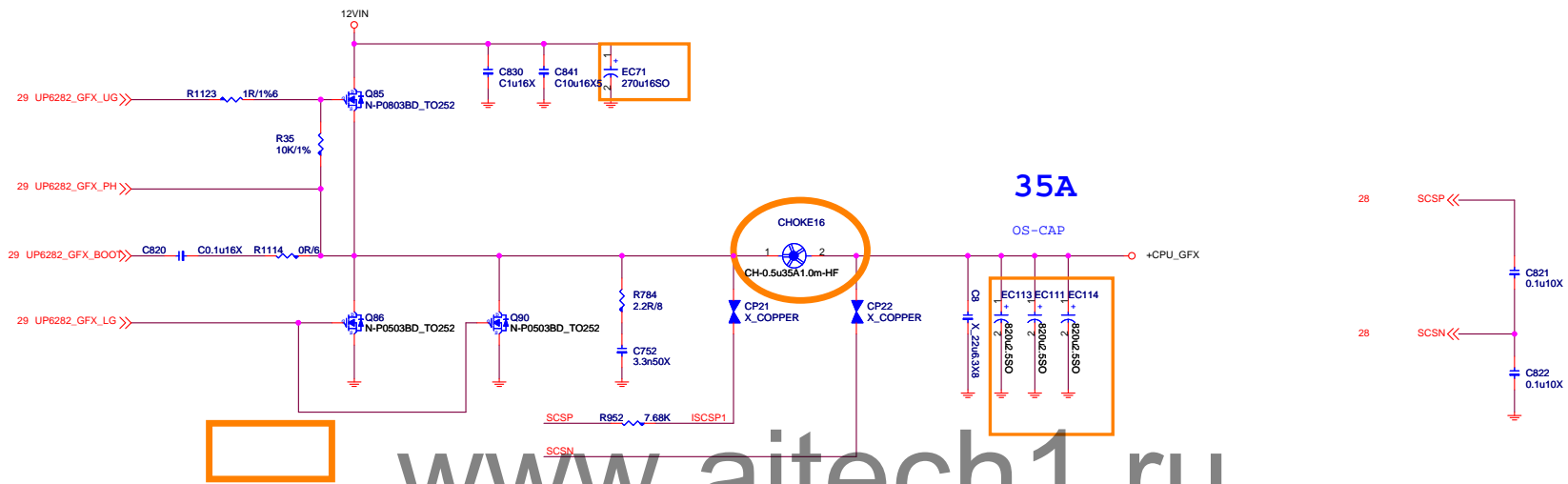
Size Custom Document Description  
VRD12 - PWM-UT501  
Date: Tuesday, May 22, 2012 Sheet 28 of 41





# CPU\_GFX:0.25-1.52

35A FOR CPU



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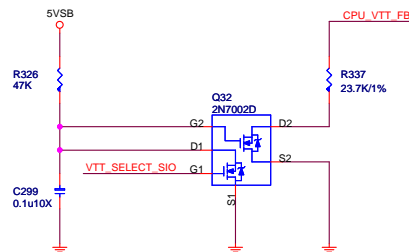
$$I_{ripple} = 1.92(v_{tt}) + 1.88(sa)$$

$$5 \times 1 = 5A > 3.8A$$


```
VTT_SELECT
0 : 1.0V
1 : 1.05V
```

3 VTT\_SELECT>>\_\_\_\_\_


suggest 1.5V  
max : 1.8V



CPU\_SA:0.925/0.85

SA Core =8.8A

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			MICRO-STAR INT'L CO.,LTD		
			MS-7808		
Size	Document Description			Rev	
Custom	CPU_SA OP+MOS 1-Phase			0A	
Date: Friday, May 11, 2012			Sheet	32	of 41

# DDR Power:1.5V

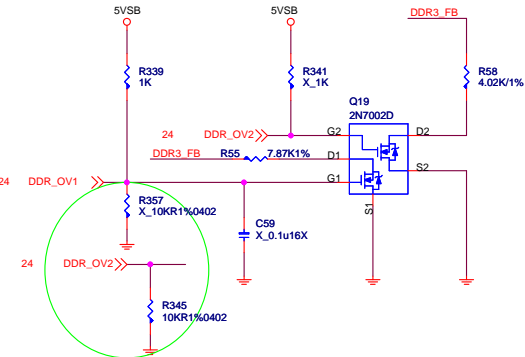
DDR3\_1.5V 4.75A+5.5A+0.5A=10.75A

4.75A FOR CPU

5.5A FOR 2DIMM

0.5A FOR DDR VTT

## DDR OV

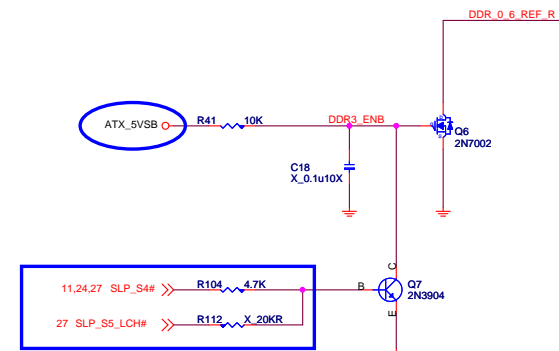


\*Default 1.5V

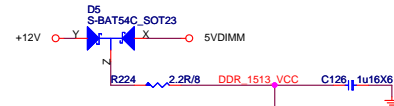
DDR_OV	1.35V	1.5V	1.65V	1.8V
DDR_OV1	Low	High	Low	High
DDR_OV2	Low	Low	High	High

DDR\_OV1 = GPIO01(S/IO)

DDR\_OV2 = GPIO02(S/IO)

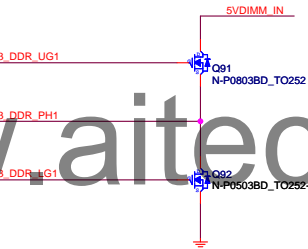


P.S. Only for meet Intel power down sequence.

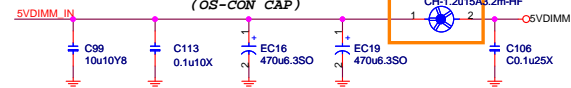


$$((R221/R226)+1)*0.6=1.5V$$

Internal 0.6

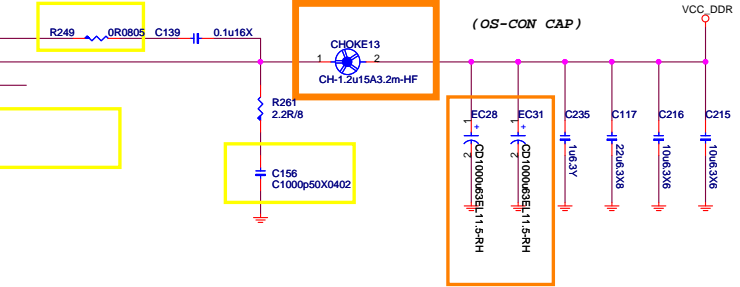


Tripple=8A  
4.7\*2\*1=9.4A>8A



## DDR3\_1.5V

(OS-CON CAP)

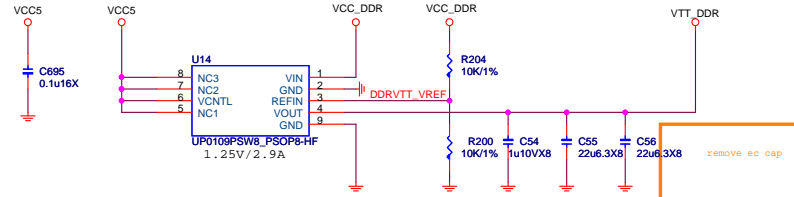


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## DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

$$0.2075A*4=0.8A$$

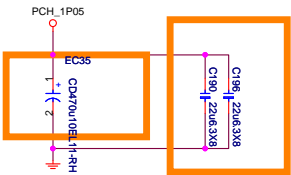


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Custom	DDR Power -UP1513 1-Phase MOS	0A
Date: Friday, May 18, 2012	Sheet 33 of 41	

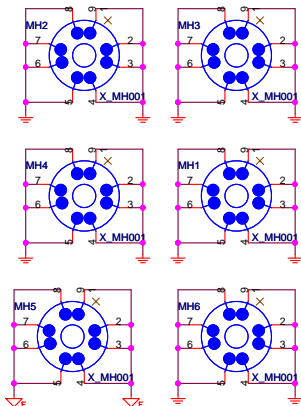
**PCH Power:1.05V**  
*PCH Core 6.2A+0.105A+0.5A+0.08A=6.935A*  
*6.2A FOR PCH*  
*0.105A FOR VCCSSC*  
*0.5A FOR VCCPLL*  
*0.08A FOR VCCDMI*



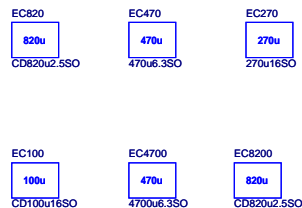
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## Mounting Holes

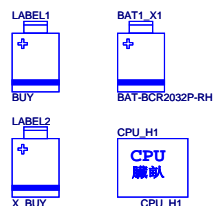
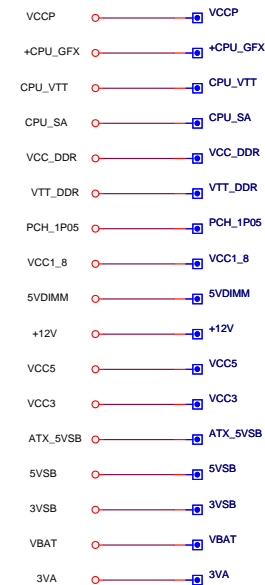
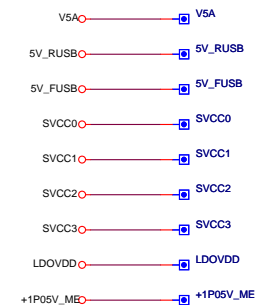


## SOLID CAP



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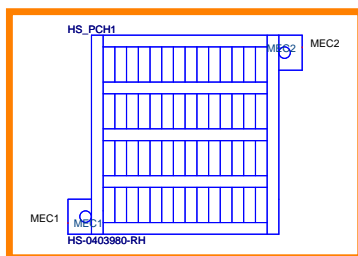
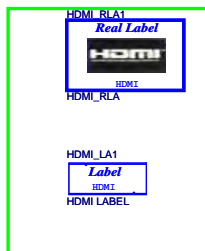
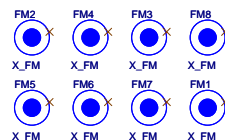
## Voltage test point



## Simulation



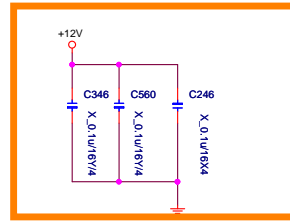
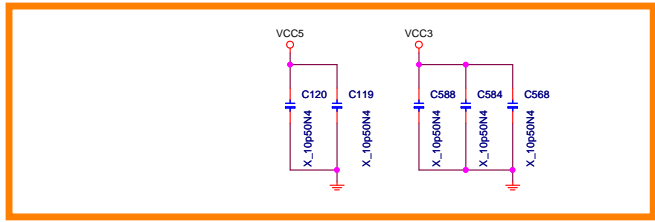
## Optical Fiducial Marks-120





EMI:cap. for signal return path

EMI



EMI

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Size  
Custom

Document Description  
EMI CAP

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0A

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